

FIG. 2

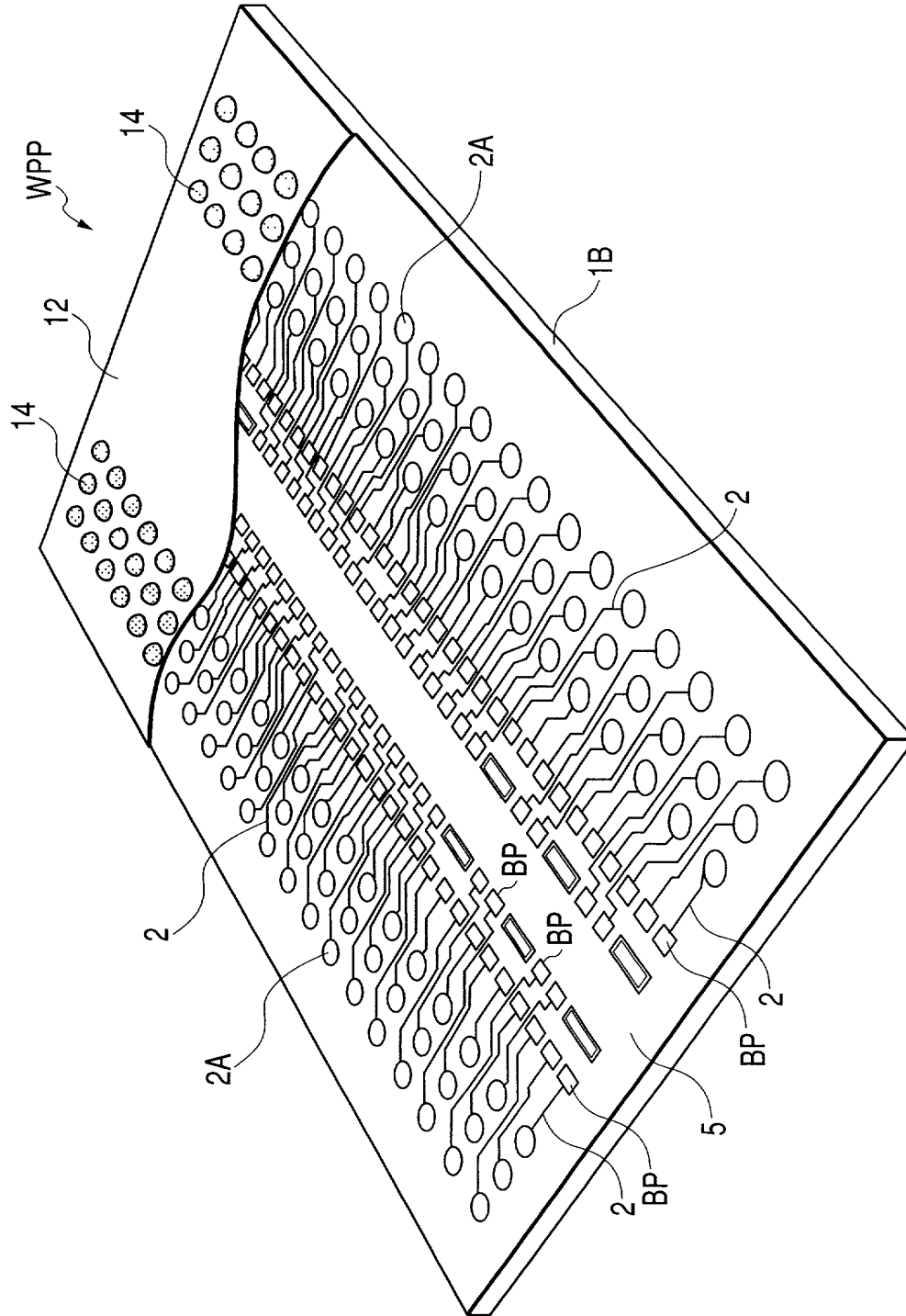


FIG. 3

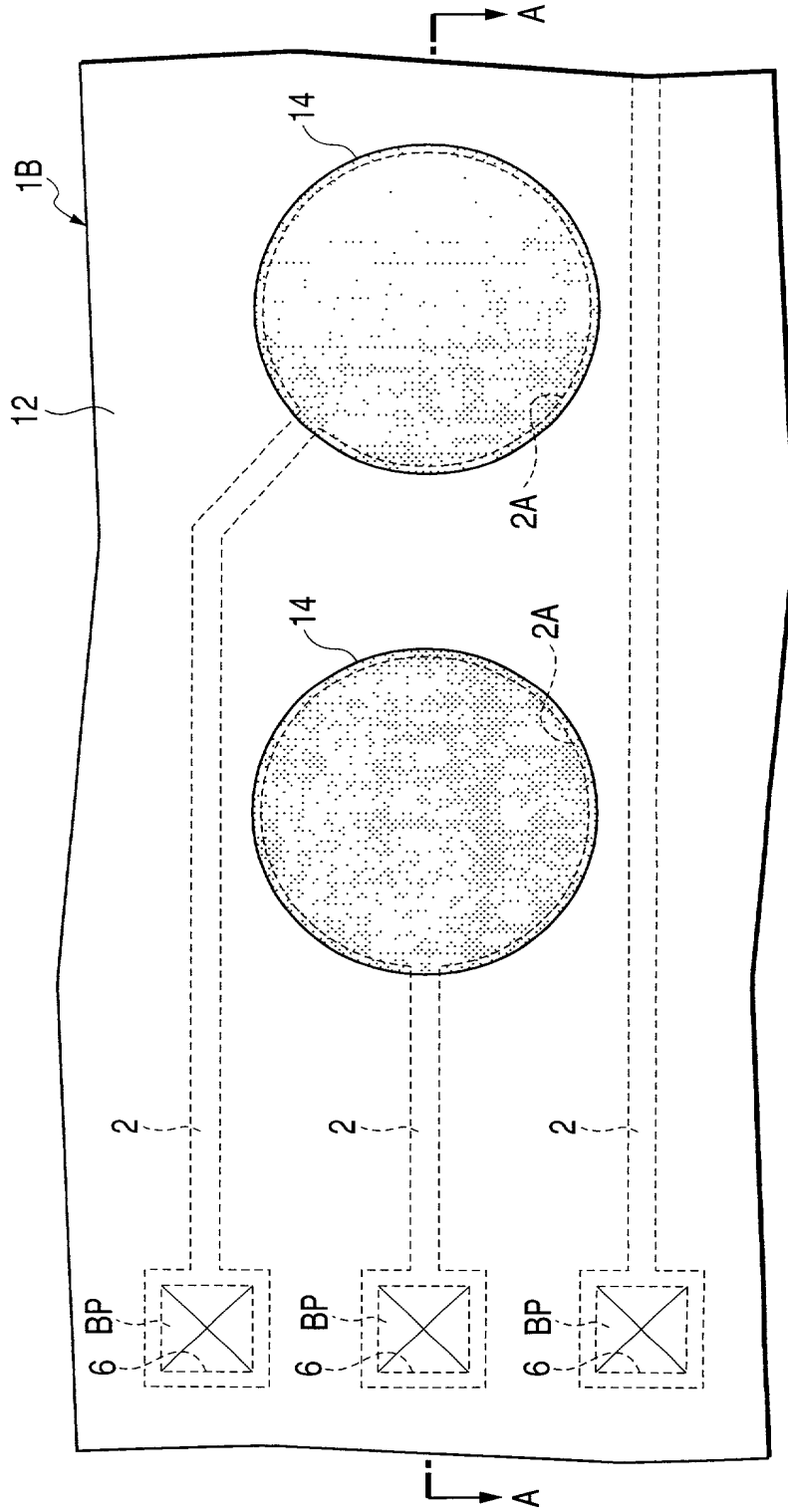


FIG. 4

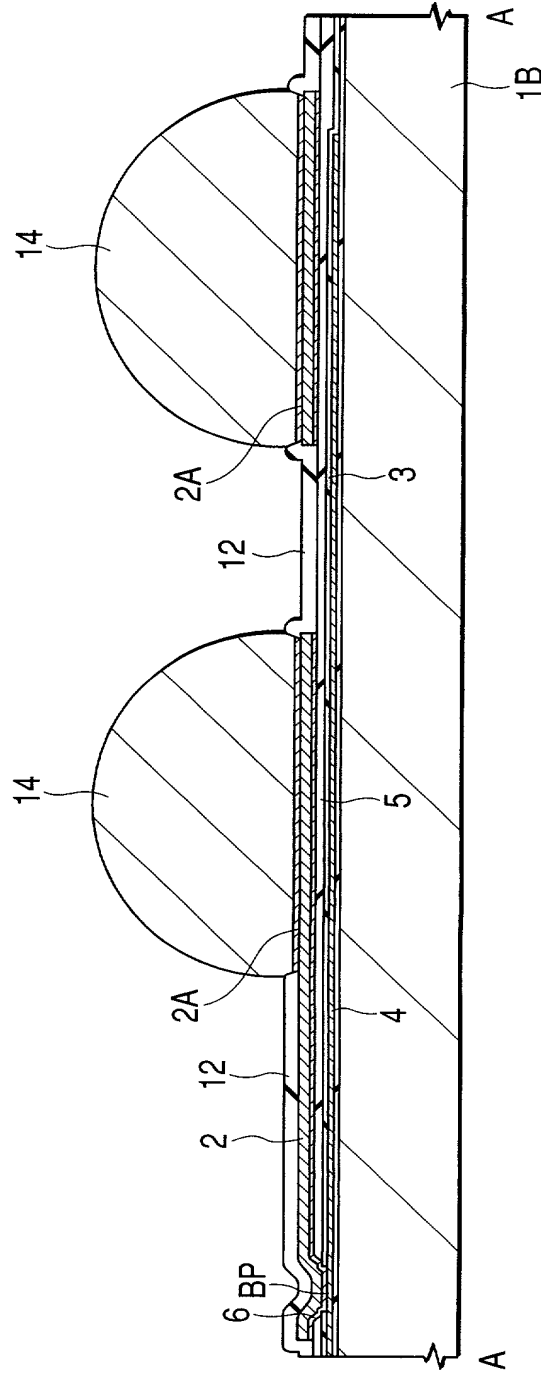


FIG. 5

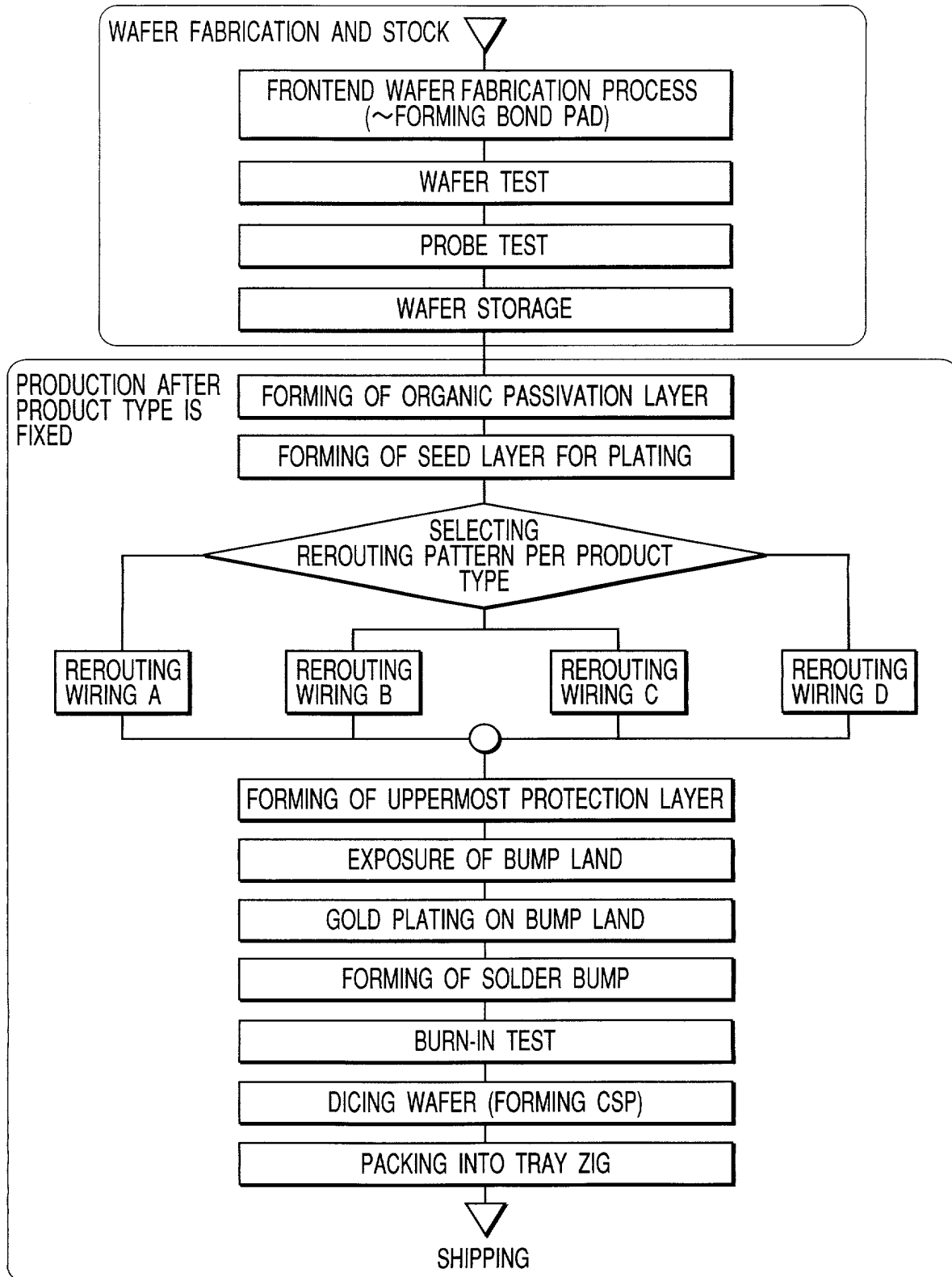


FIG. 6

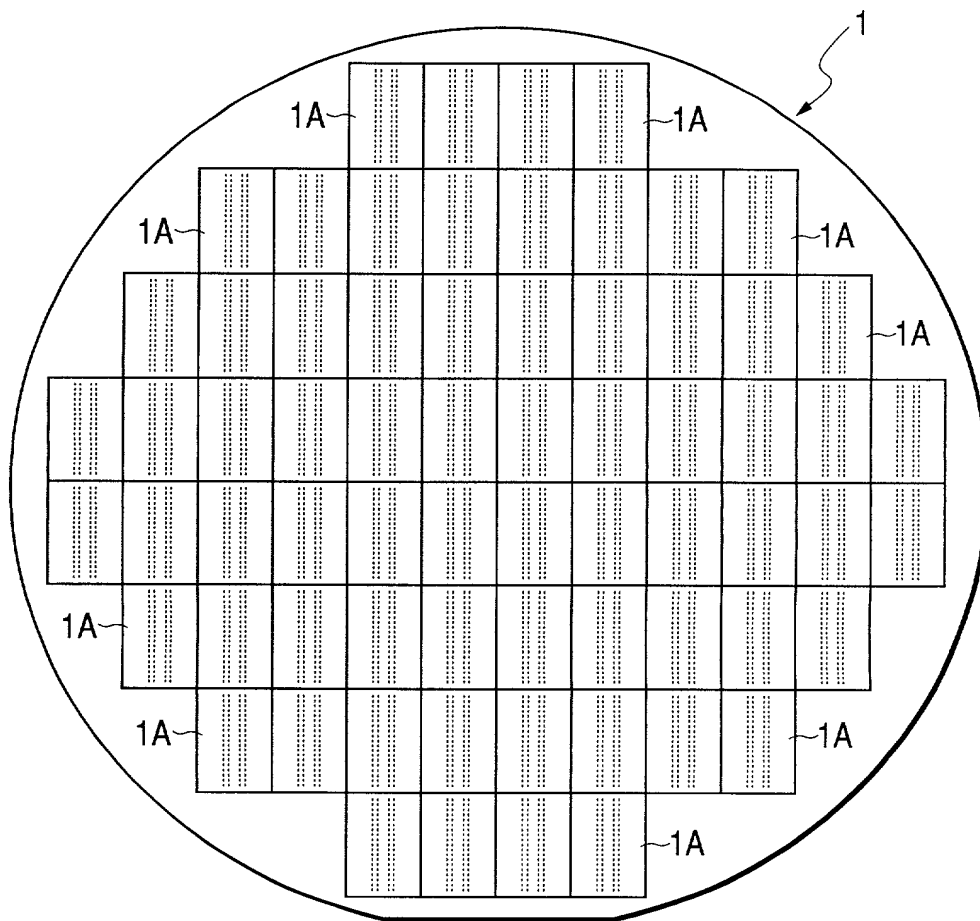


FIG. 7

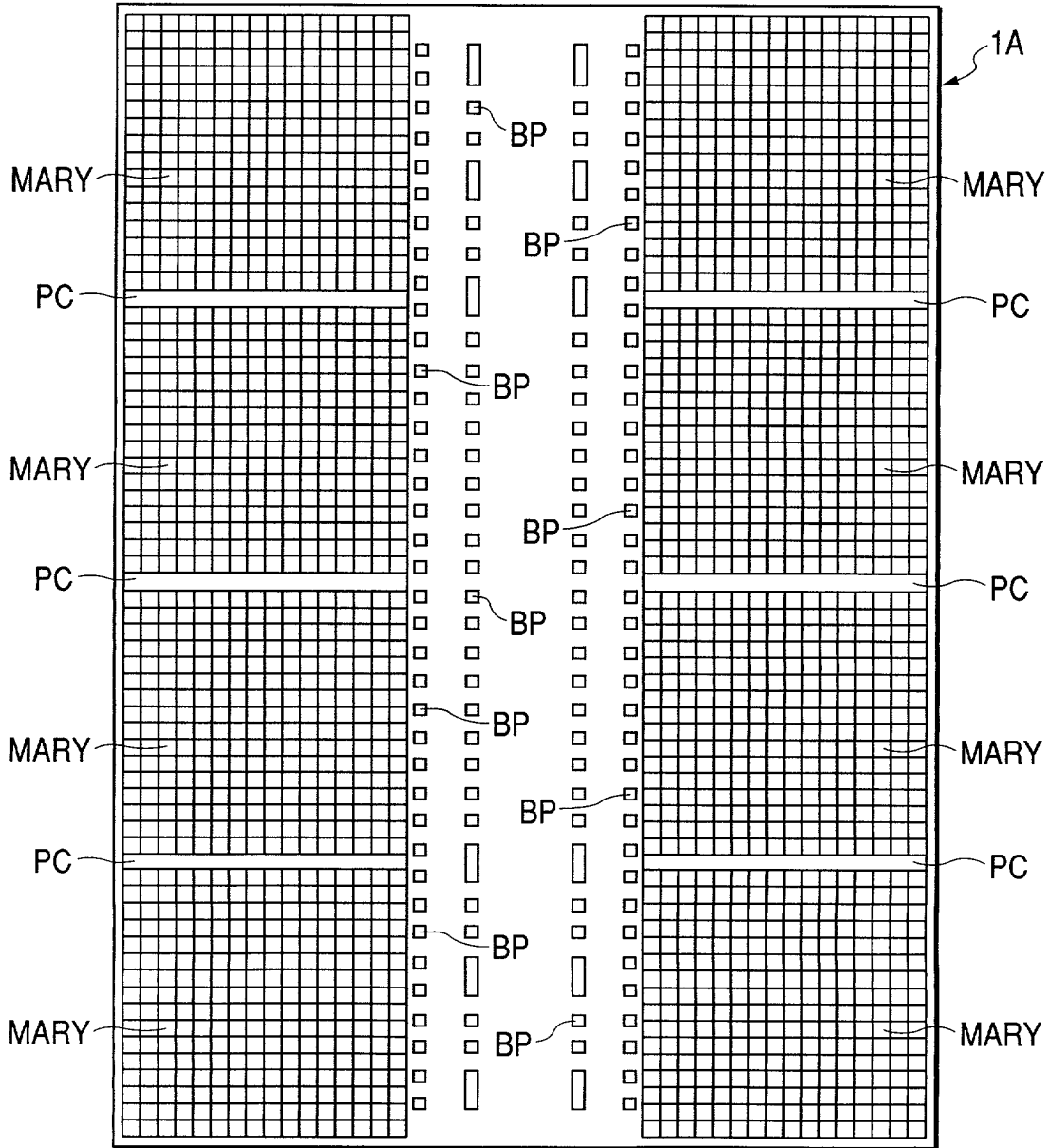


FIG. 8

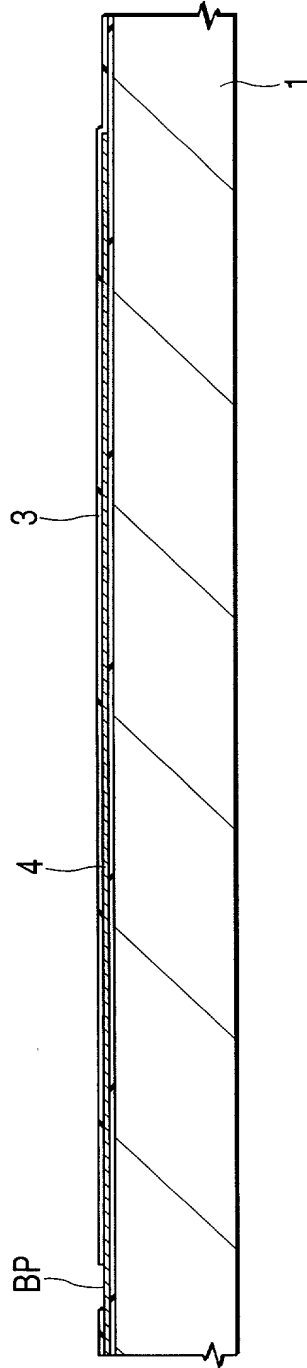


FIG. 9

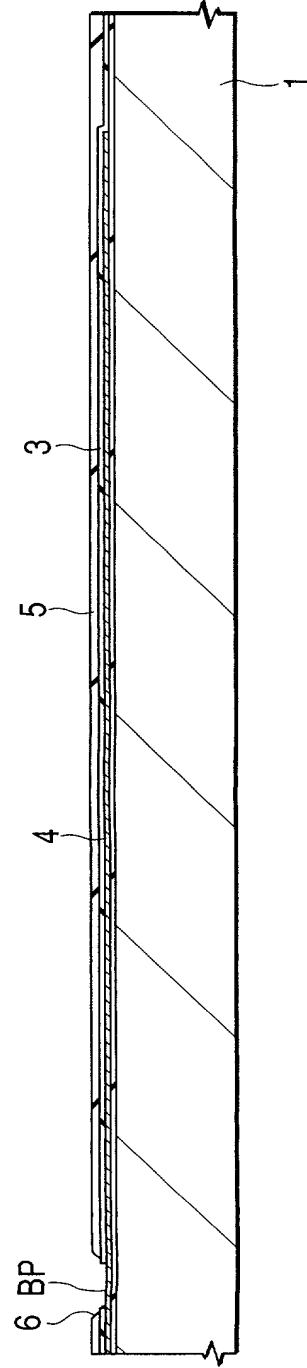


FIG. 10

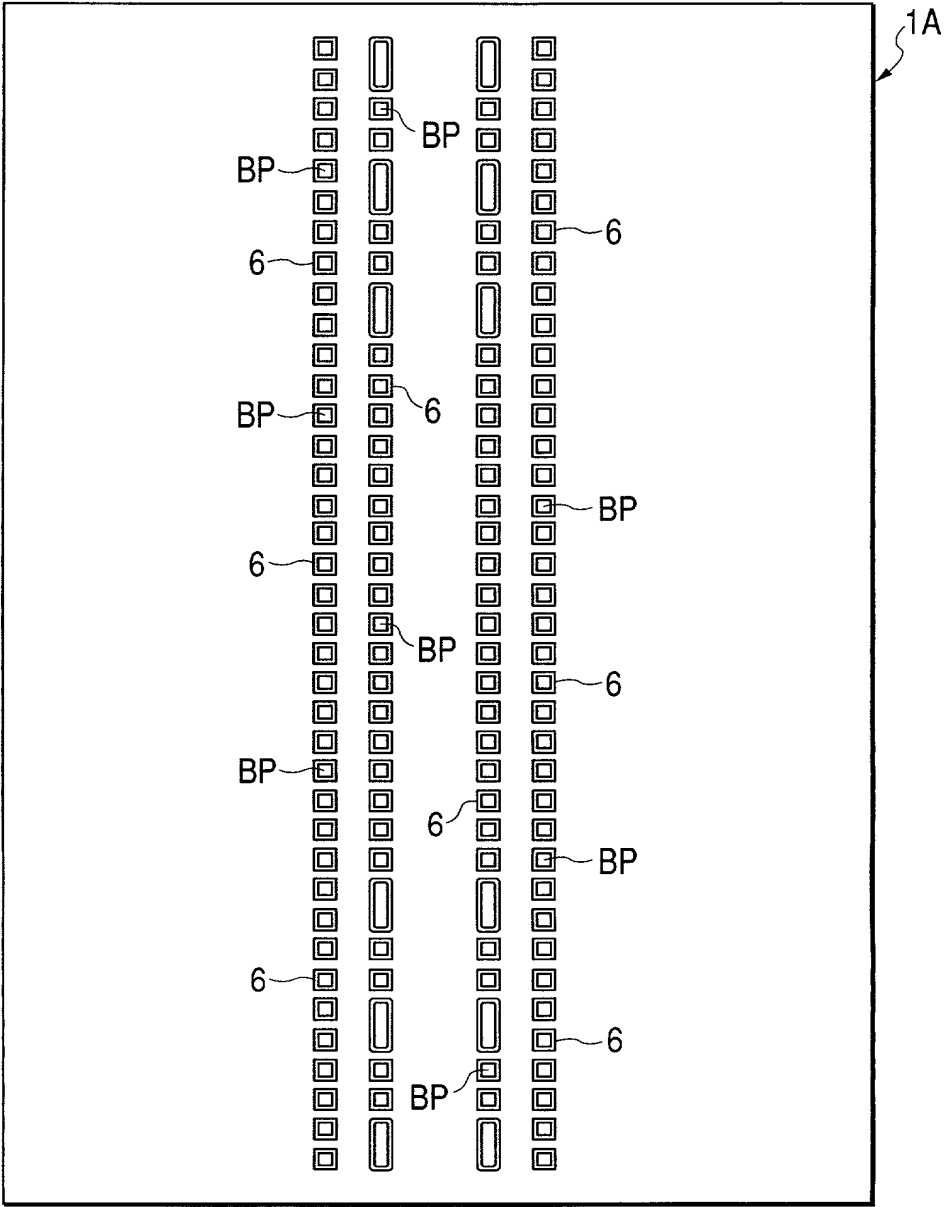
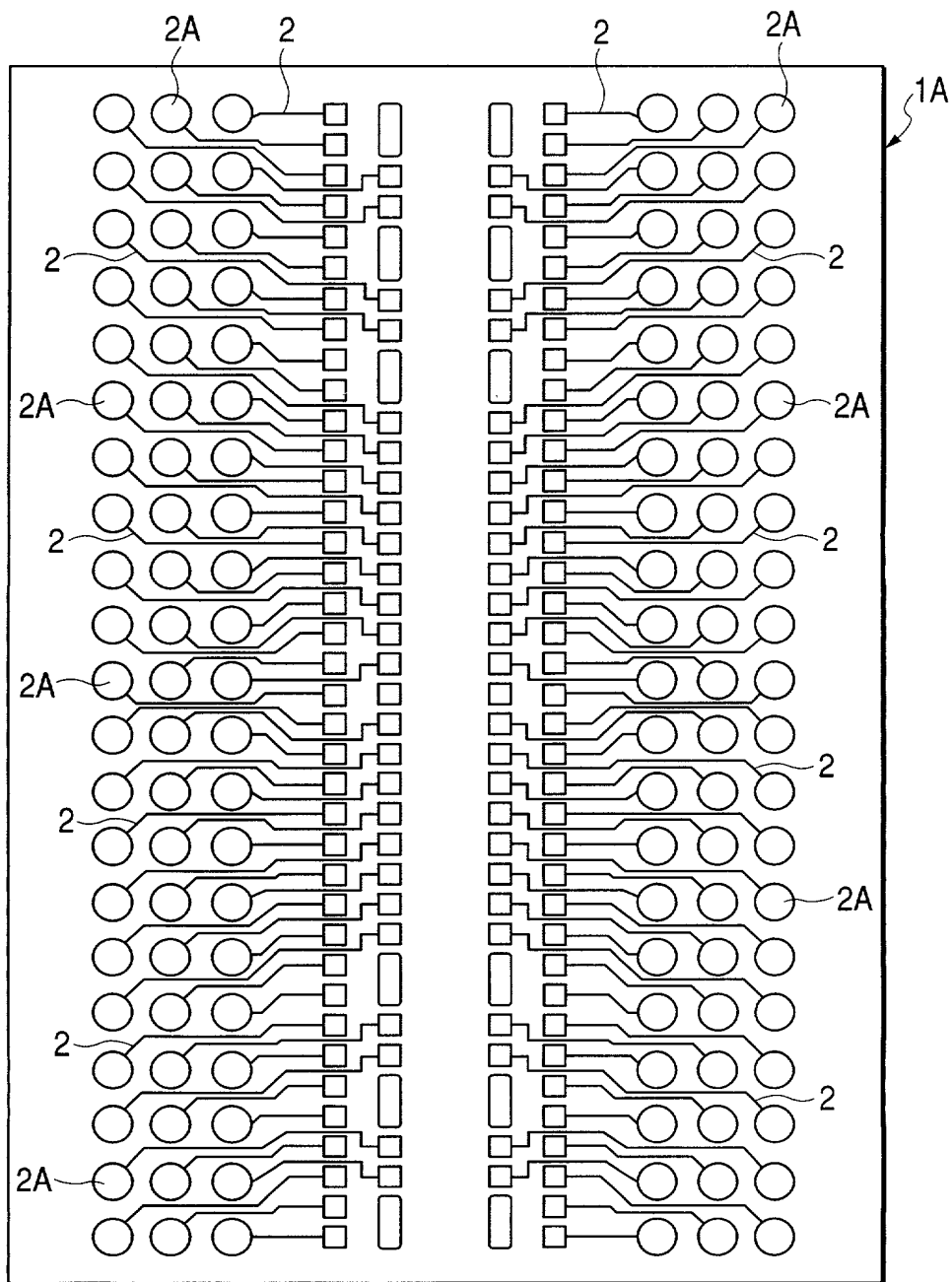


FIG. 14

LIST OF INVENTORS' NAMES AND ADDRESSES

Toshio MIYAMOTO, Kokubunji, JAPAN;

Ichiro ANJO, Koganei, JAPAN;

Asao NISHIMURA, Koganei, JAPAN;

Mitsuaki KATAGIRI, Nishi-Tokyo, JAPAN;

Yuji SHIRAI, Hamura, JAPAN;

Yoshihide YAMAGUCHI, Fujisawa, JAPAN.

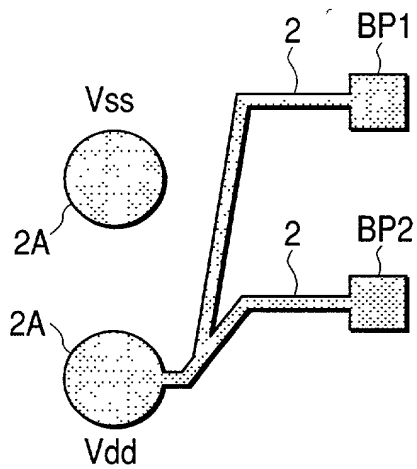
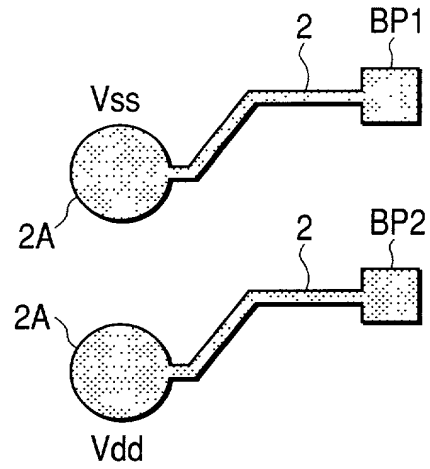
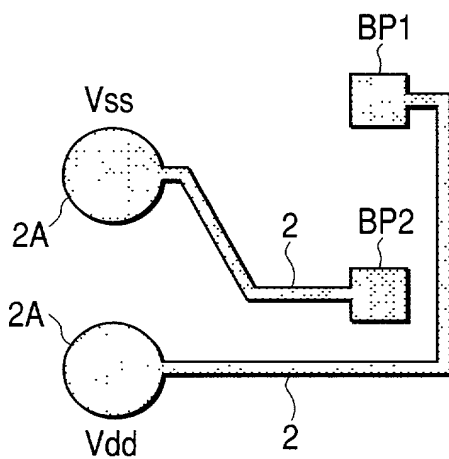
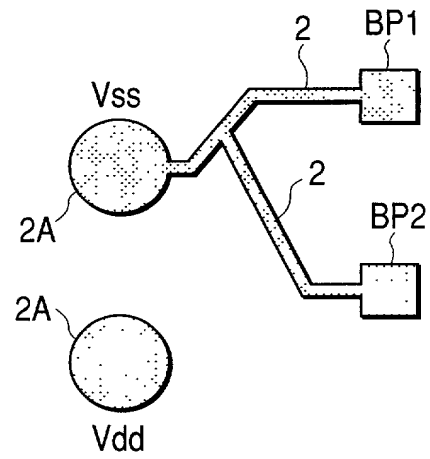
FIG. 15(a)*FIG. 15(c)**FIG. 15(b)**FIG. 15(d)*

FIG. 16

FUNCTION	PAD		BIT STRUCTURE	ACTION MODE	
	BP1	BP2		DDR	SYNCHRONOUS
FUNCTION 1	Vdd	Vdd	×32Bit	○	—
FUNCTION 2	Vdd	Vss	×32Bit	—	○
FUNCTION 3	Vss	Vdd	×64Bit	○	—
FUNCTION 4	Vss	Vss	×64Bit	—	○

FIG. 17

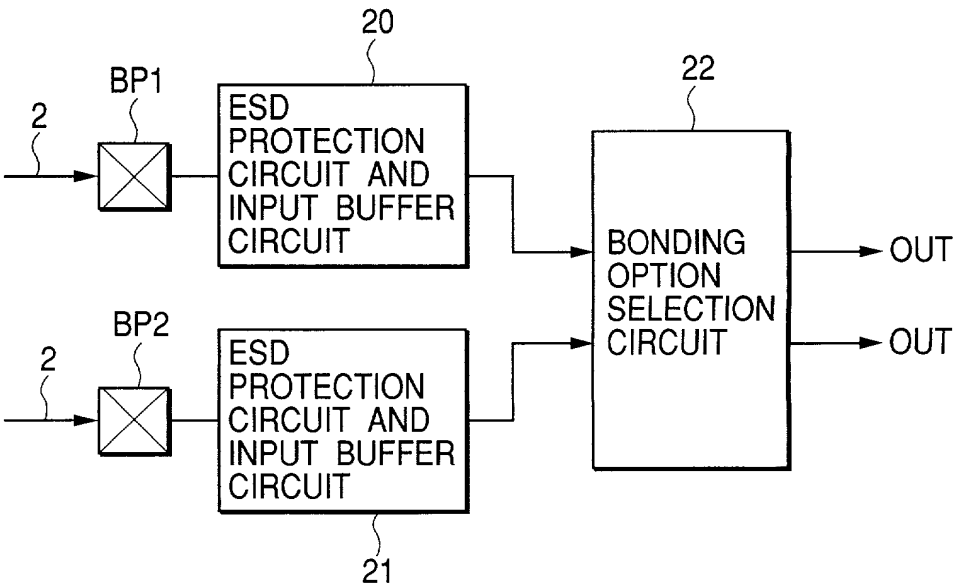


FIG. 18(a)

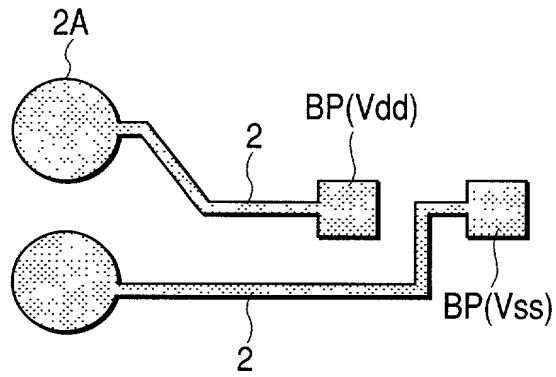


FIG. 18(b)

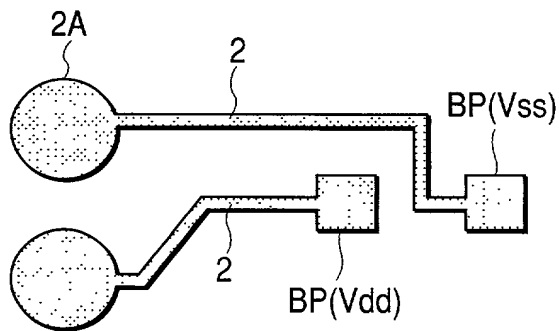


FIG. 19

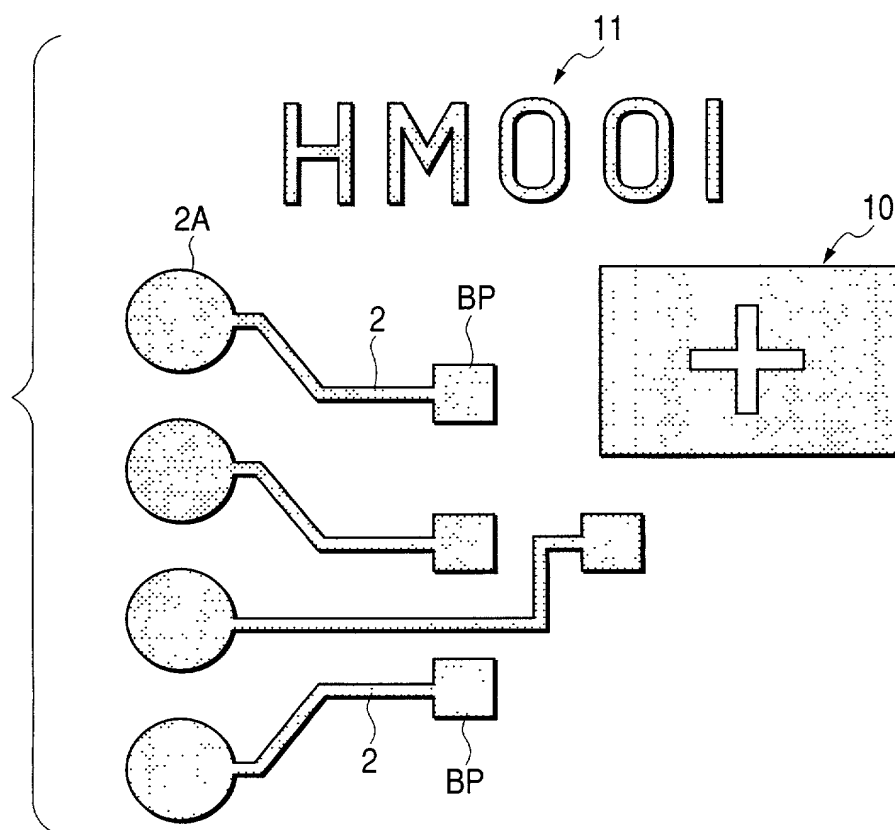


FIG. 20

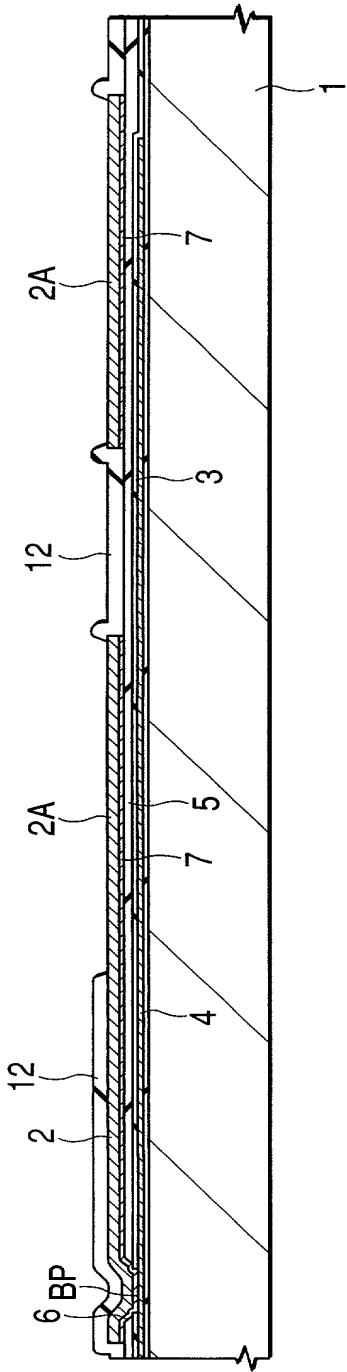


FIG. 21

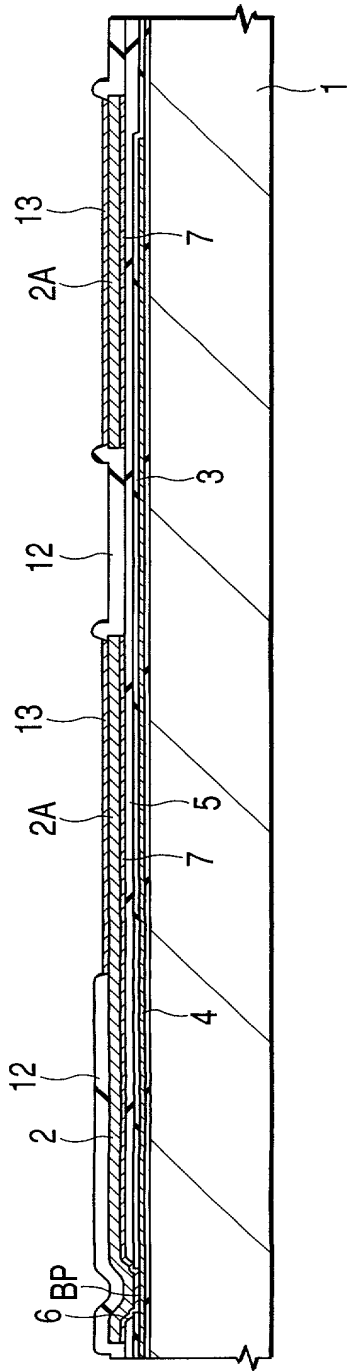


FIG. 22

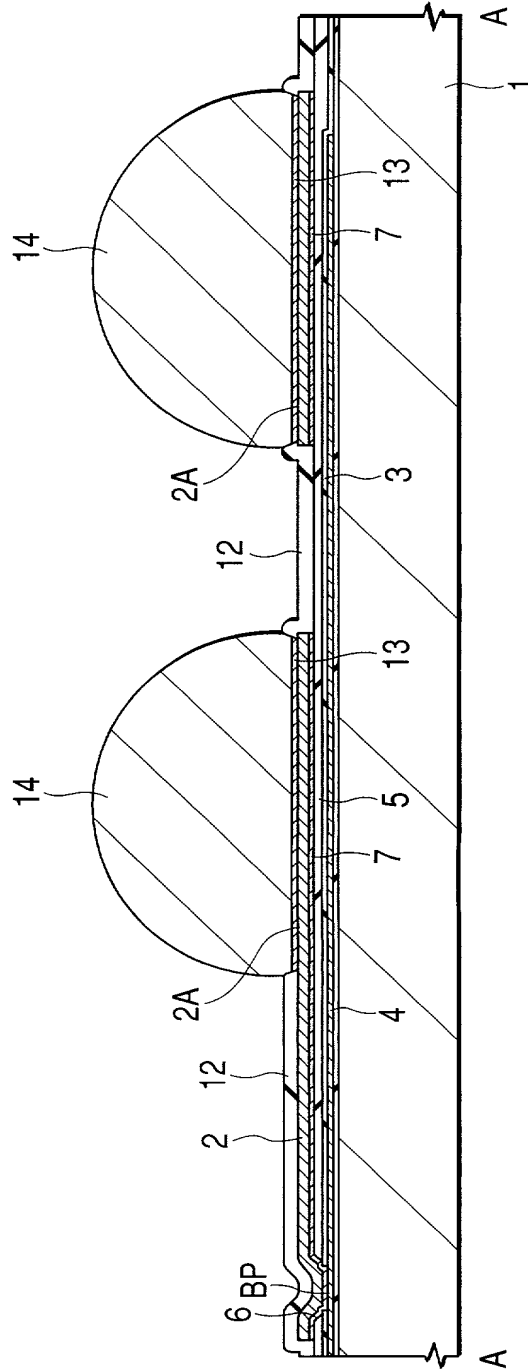


FIG. 23

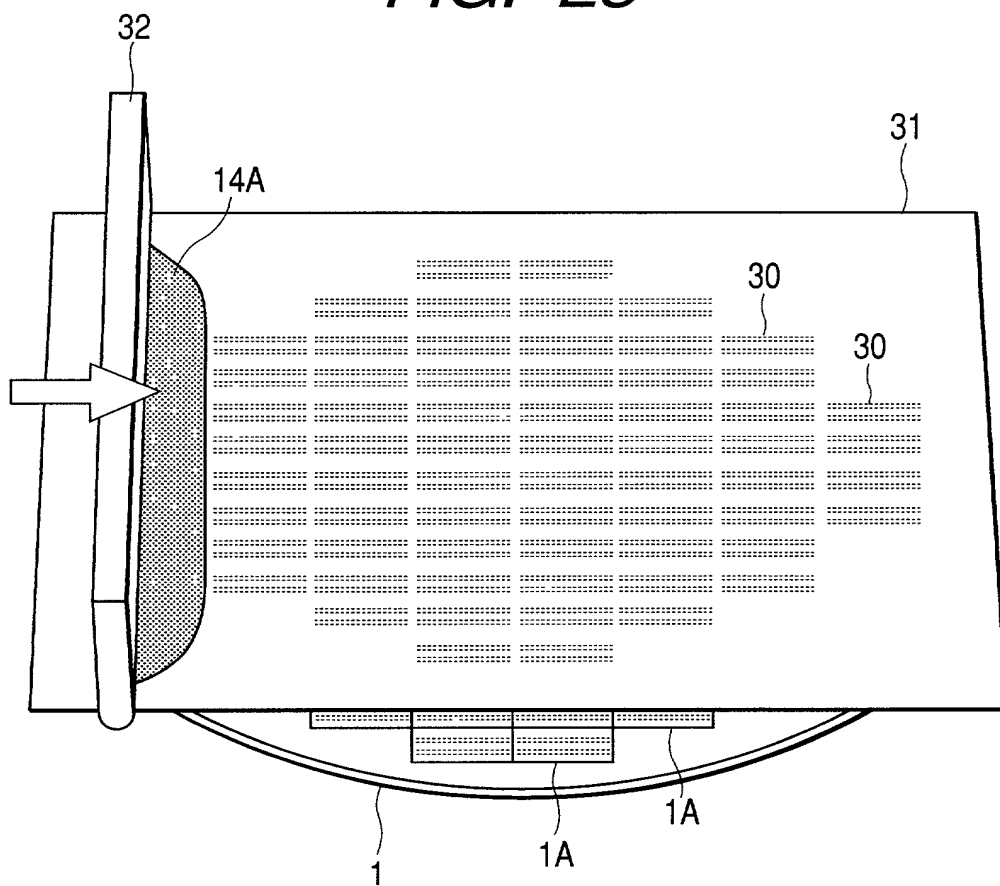


FIG. 24

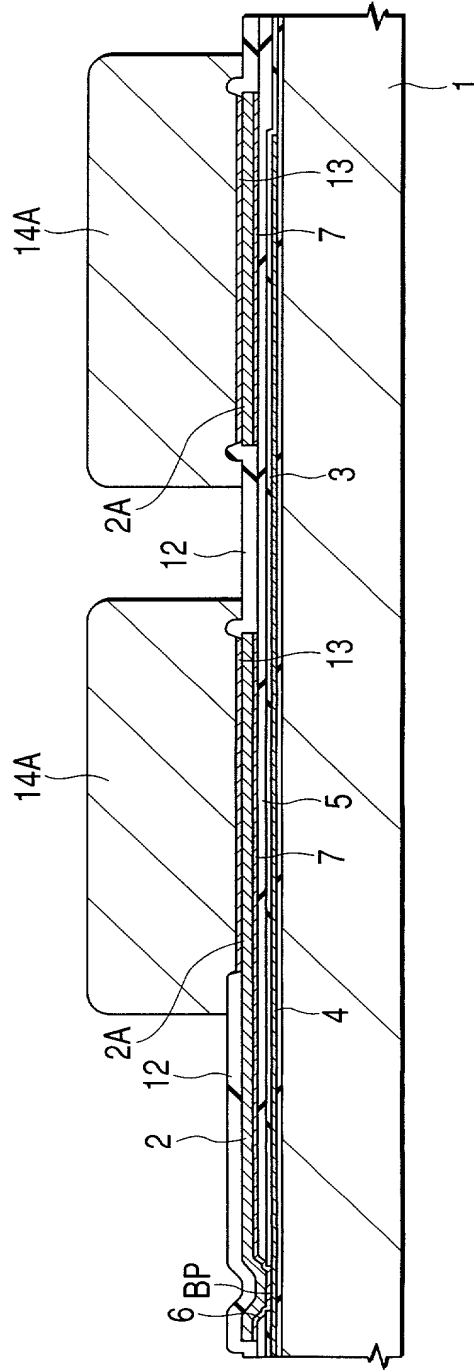


FIG. 25

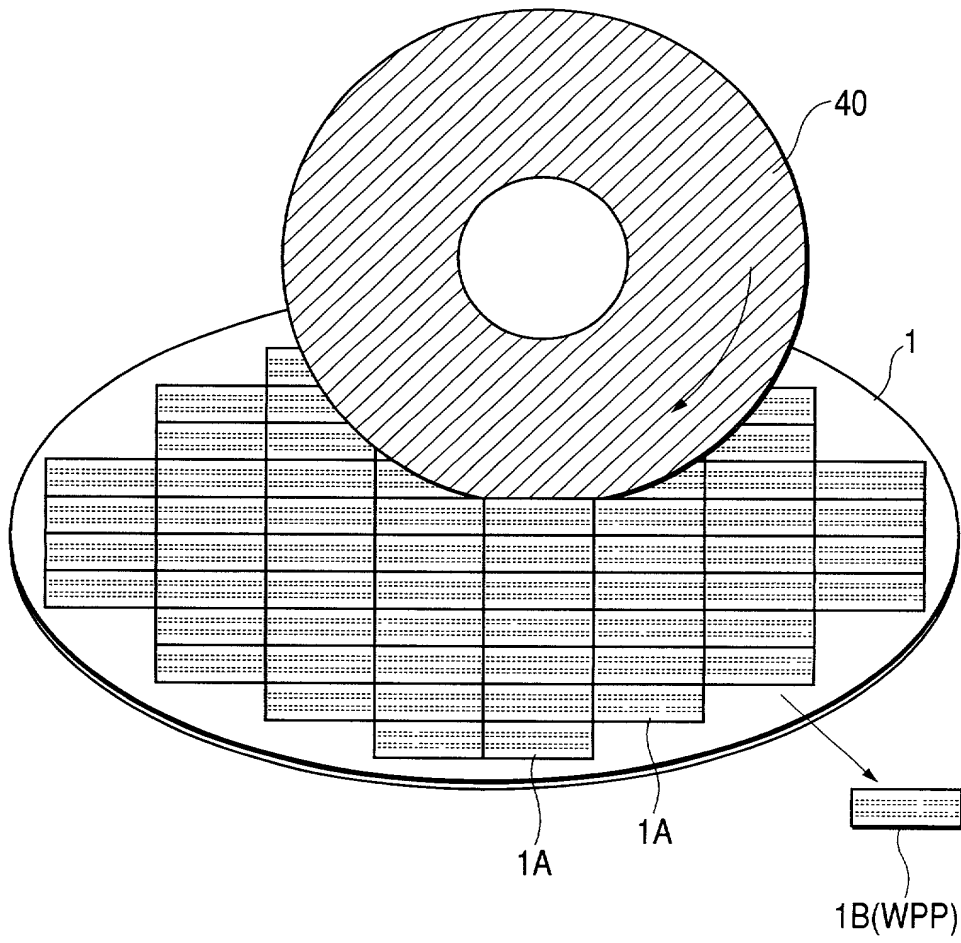


FIG. 26

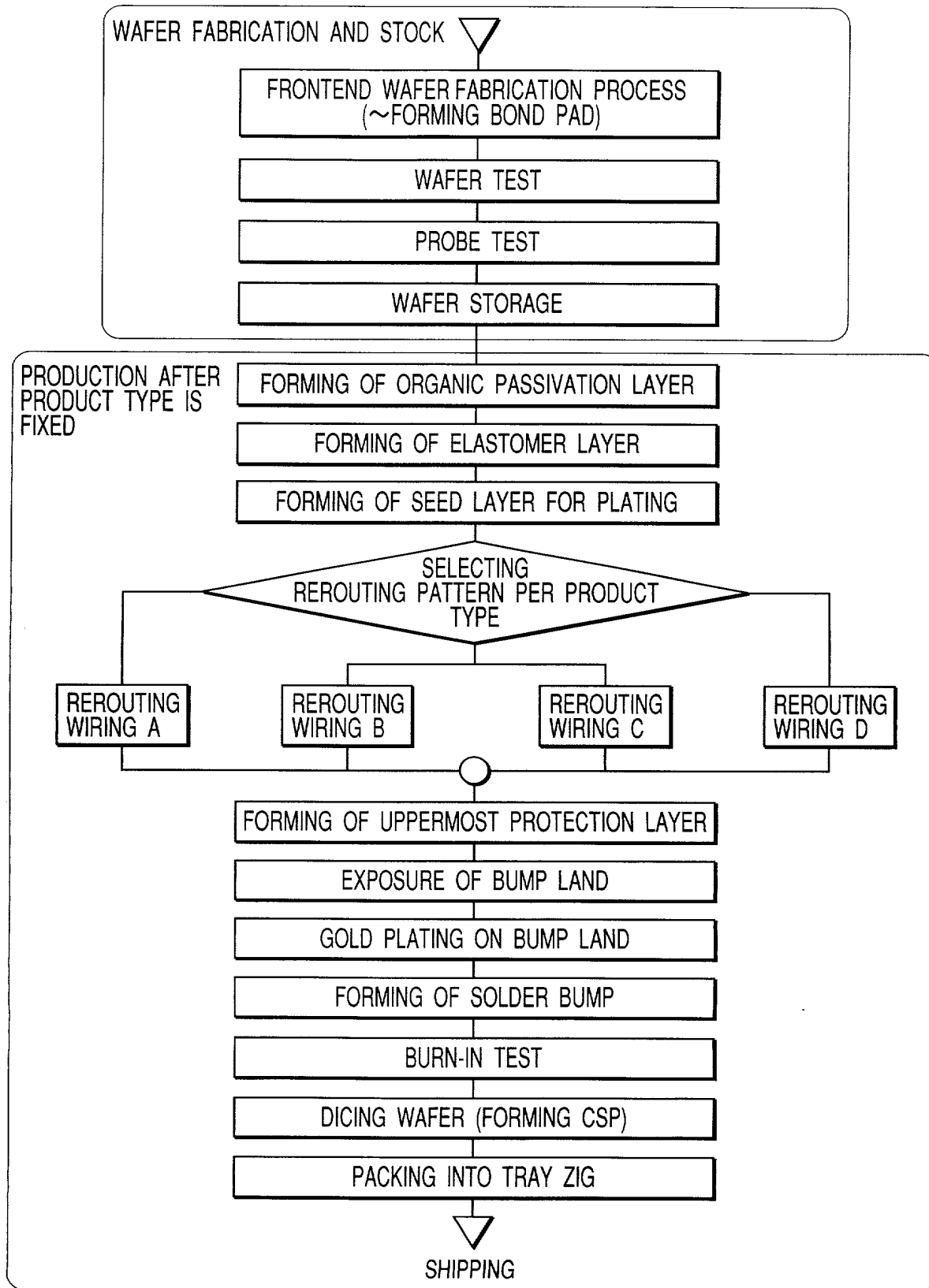


FIG. 27

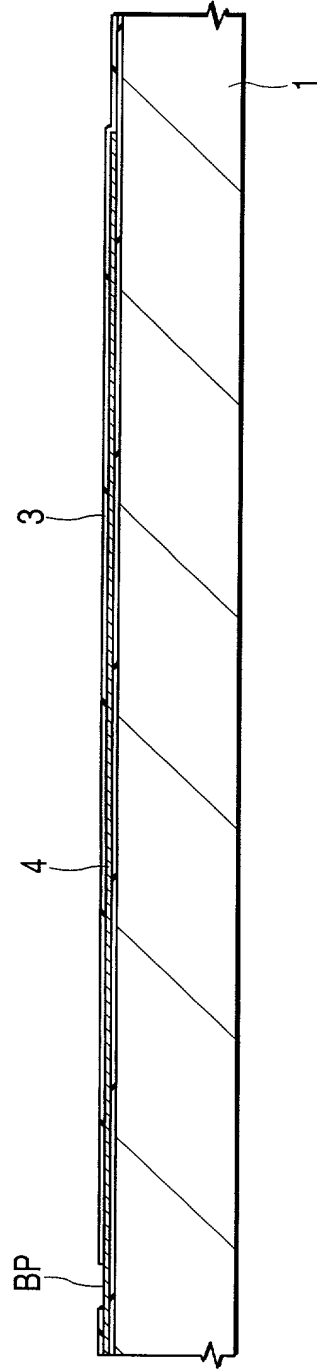


FIG. 28

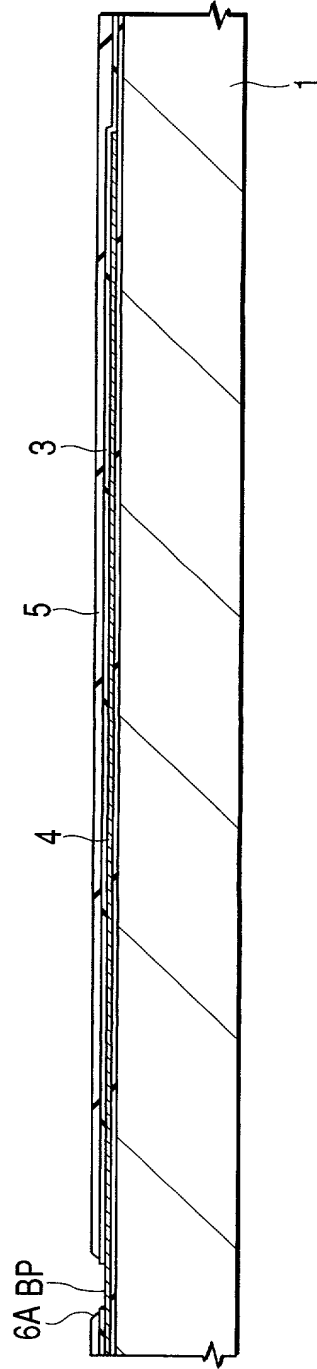


FIG. 29

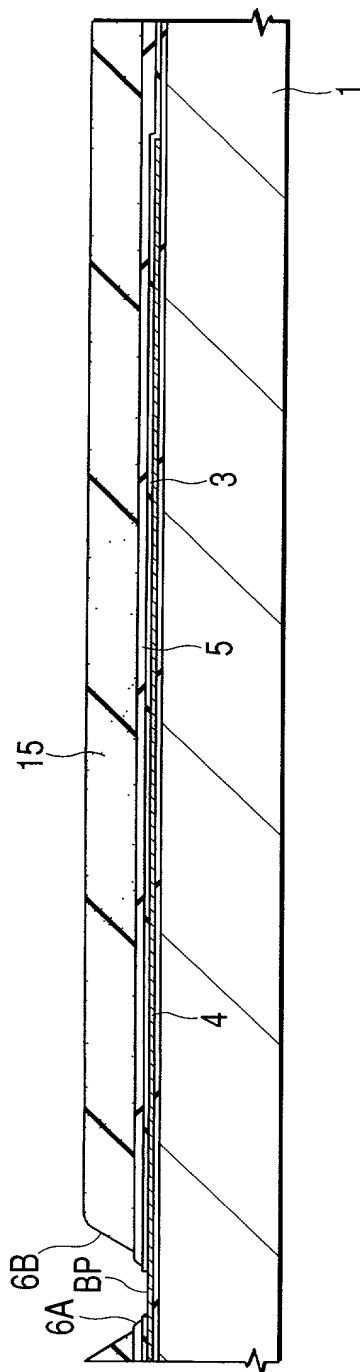


FIG. 30

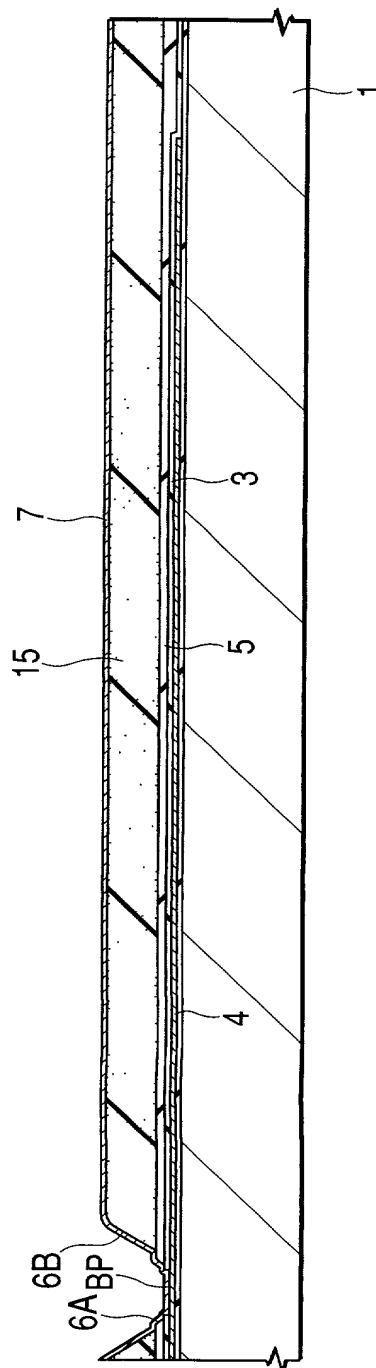


FIG. 31

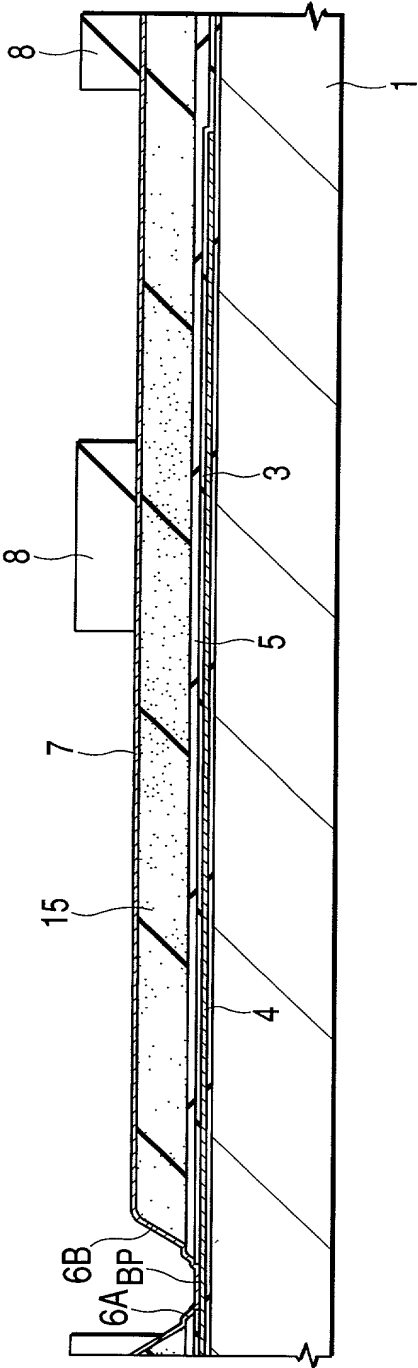


FIG. 32

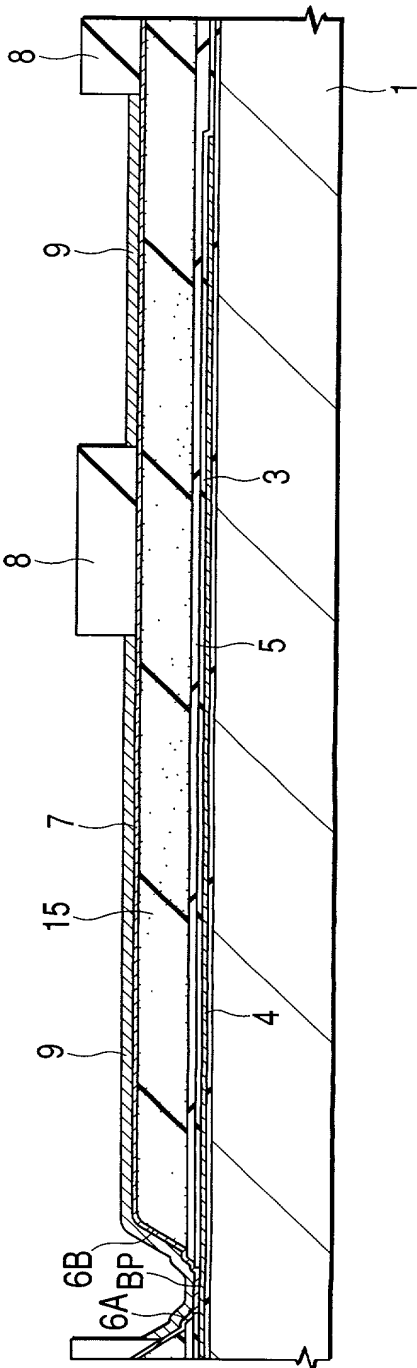


FIG. 35

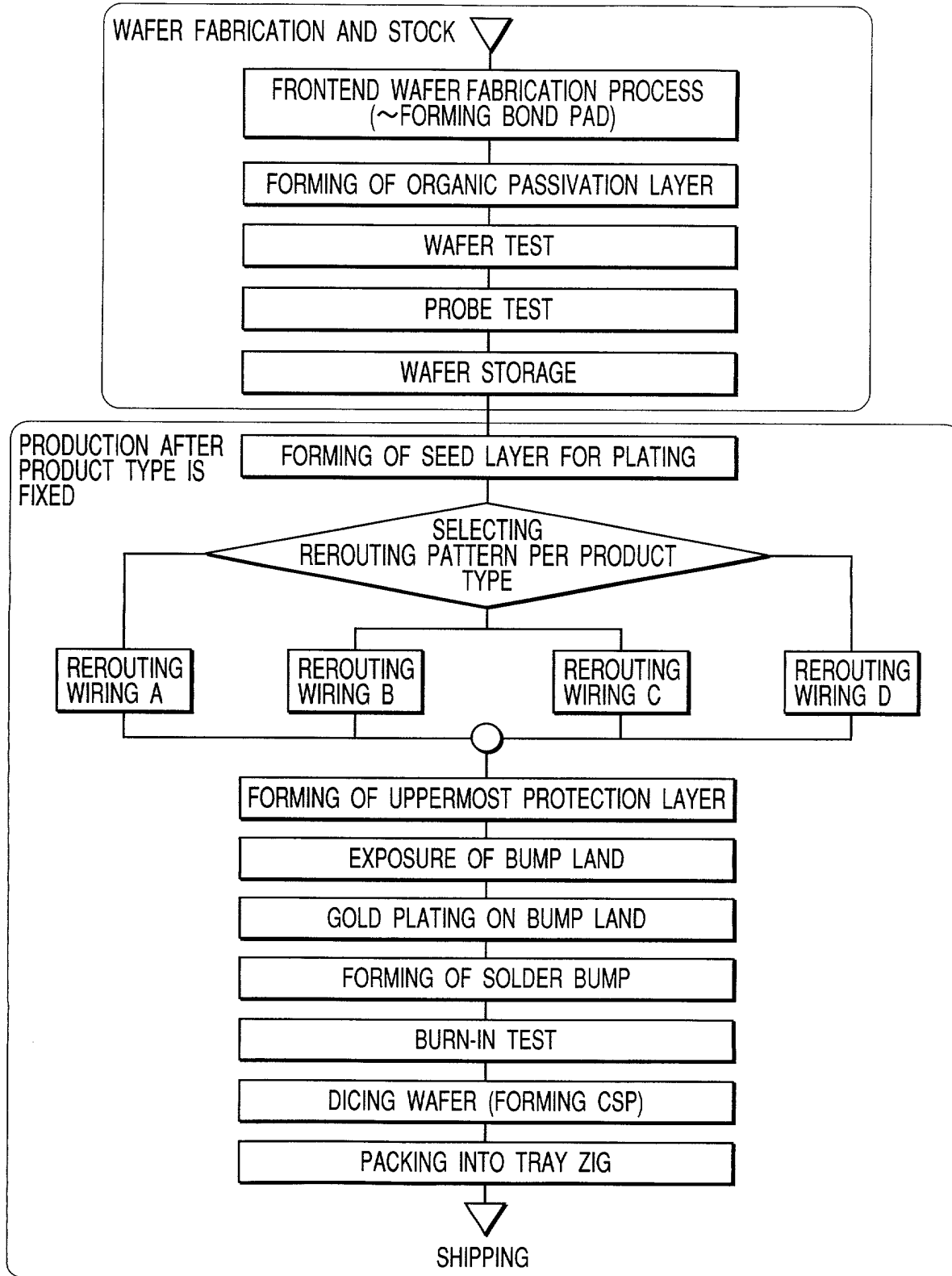


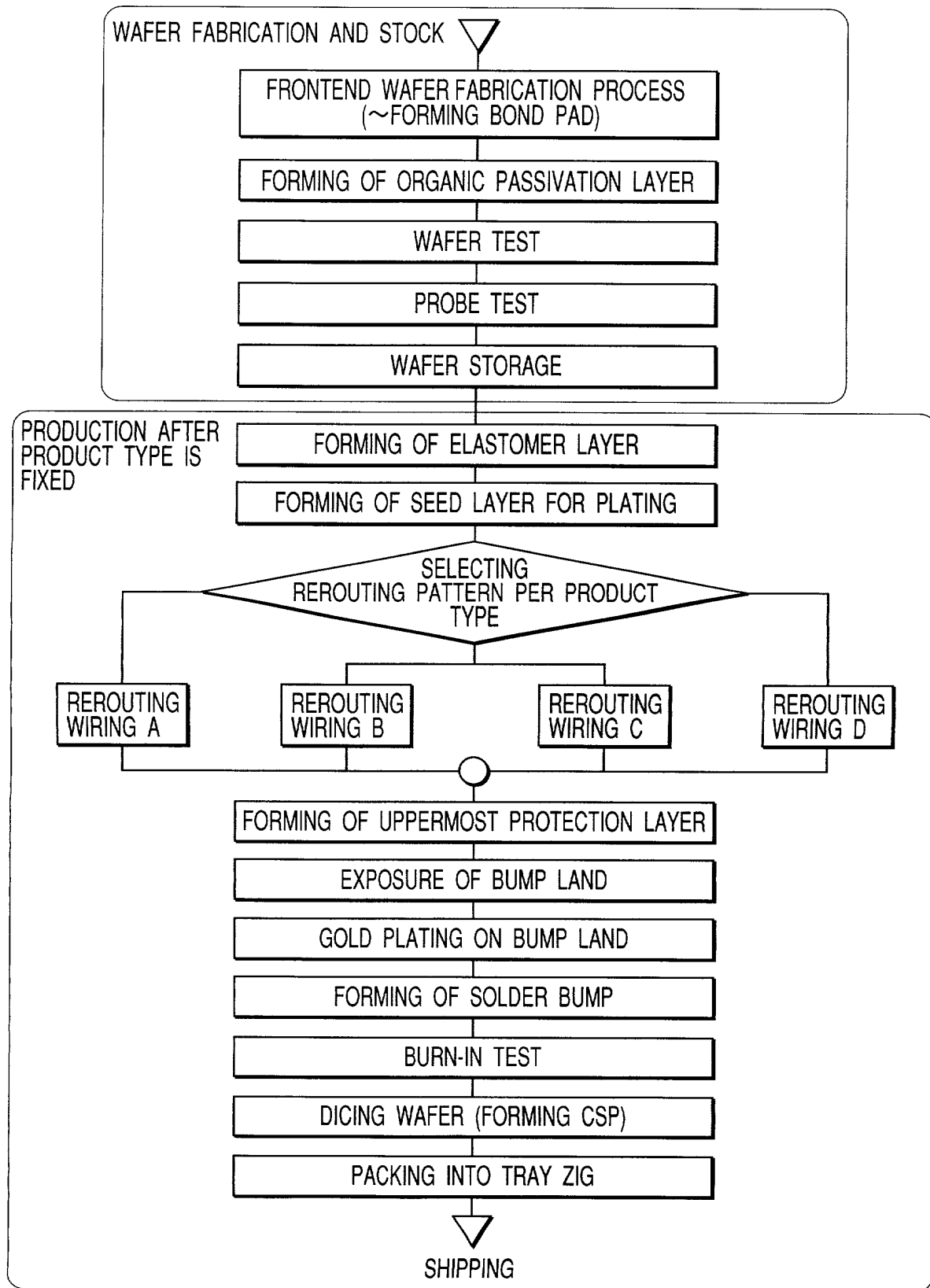
FIG. 36

FIG. 37

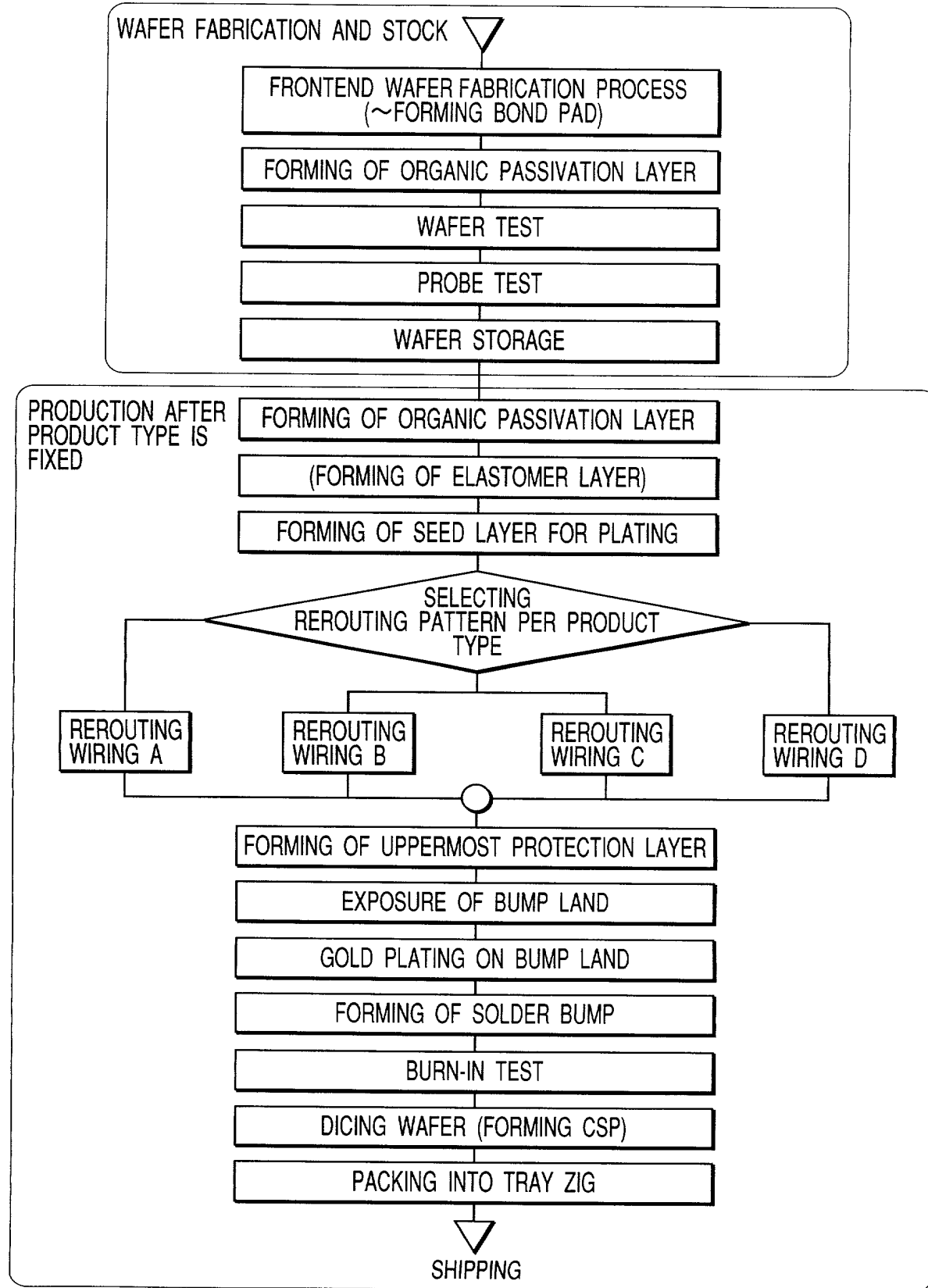


FIG. 39

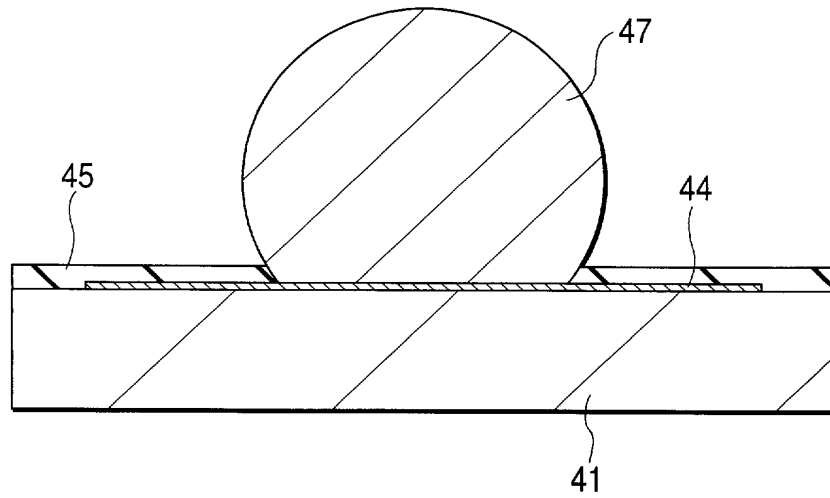


FIG. 40

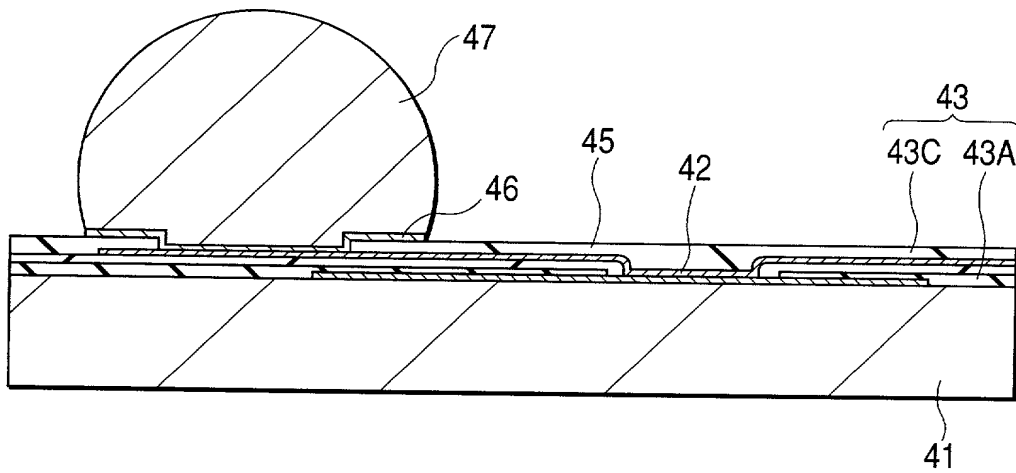


FIG. 41

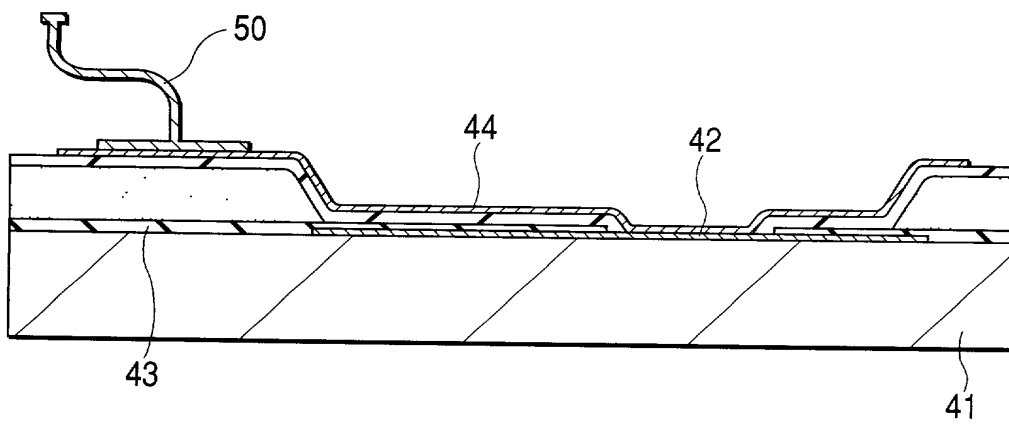


FIG. 42

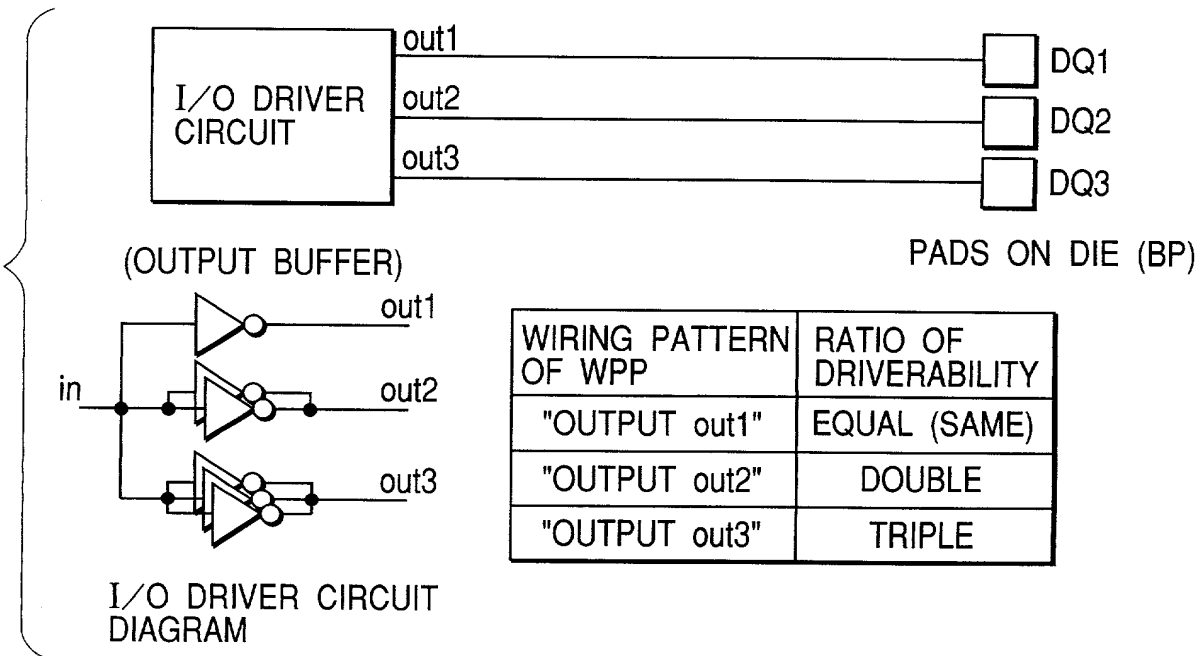


FIG. 43

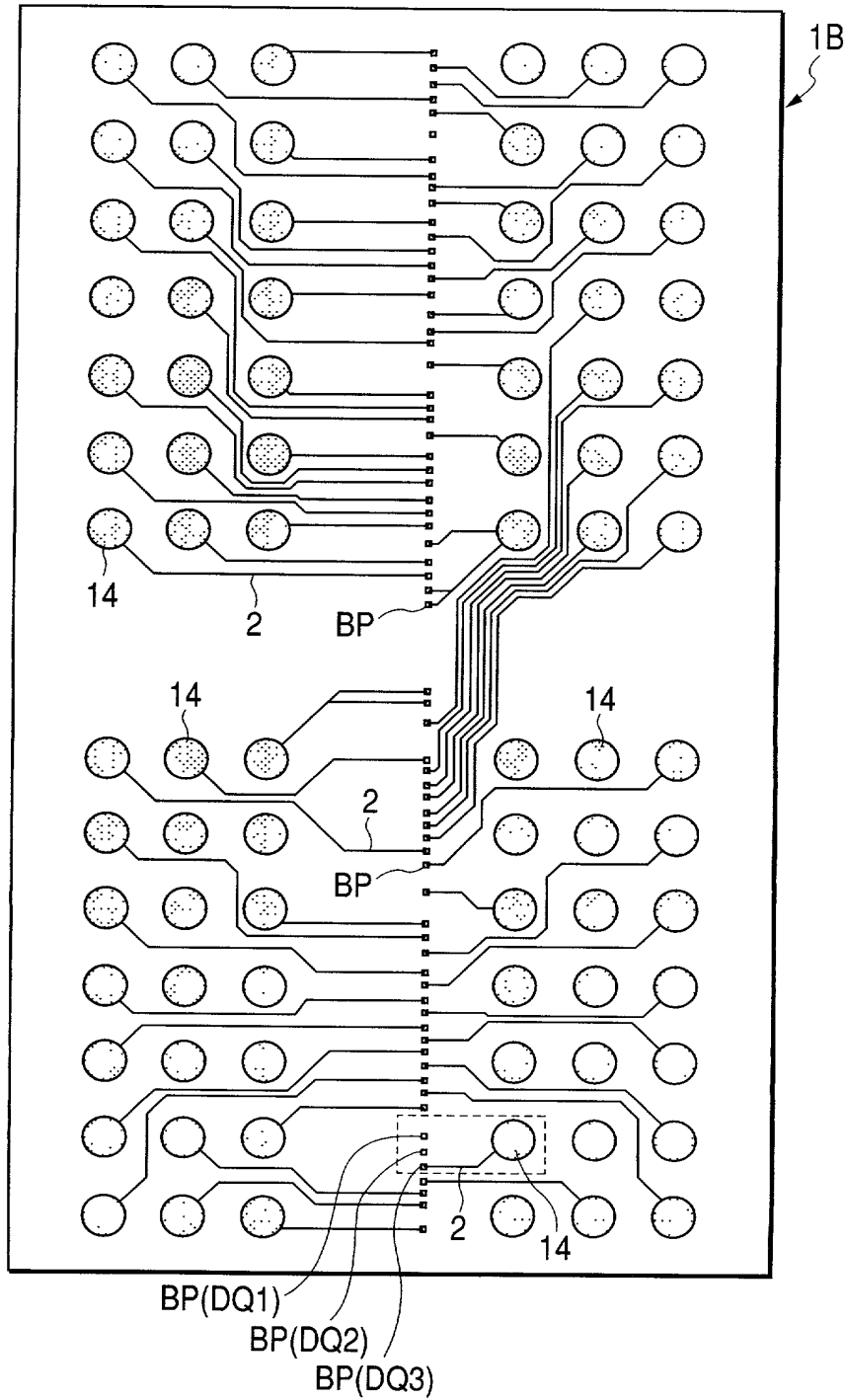


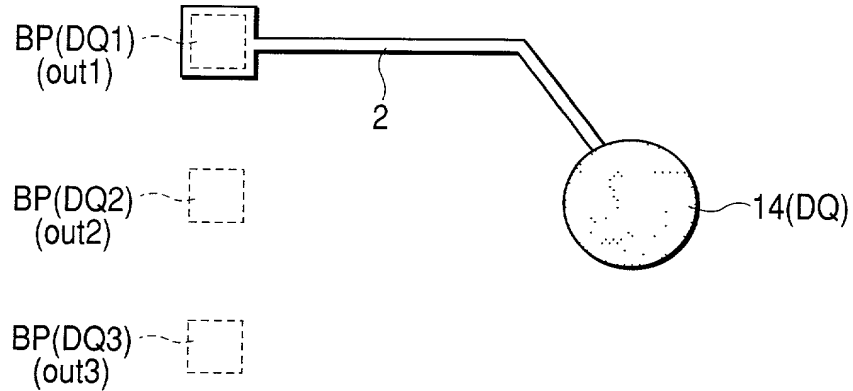
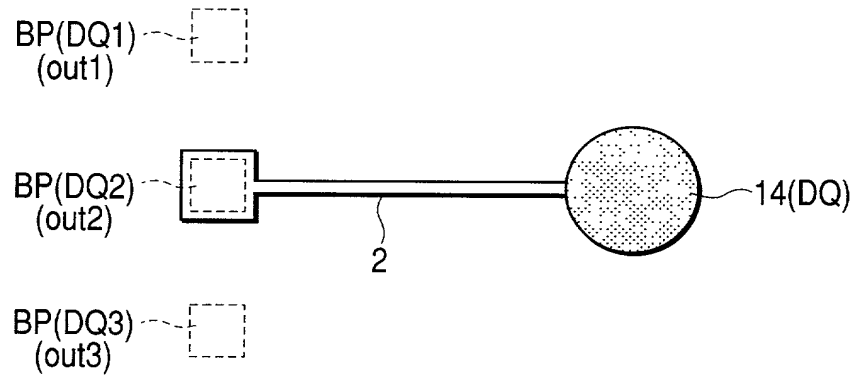
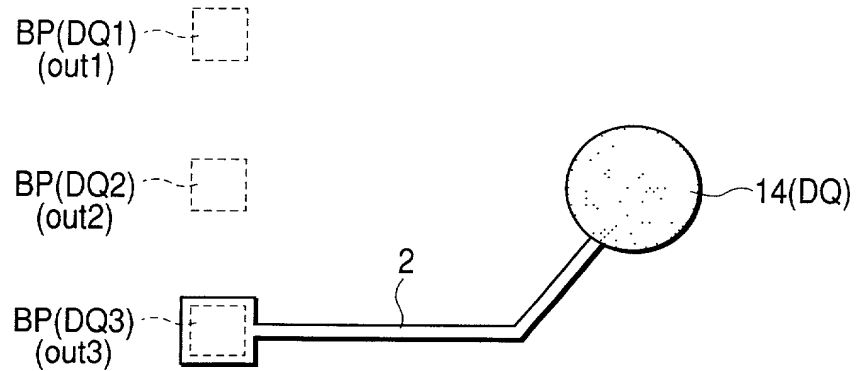
FIG. 44(a)**FIG. 44(b)****FIG. 44(c)**

FIG. 45

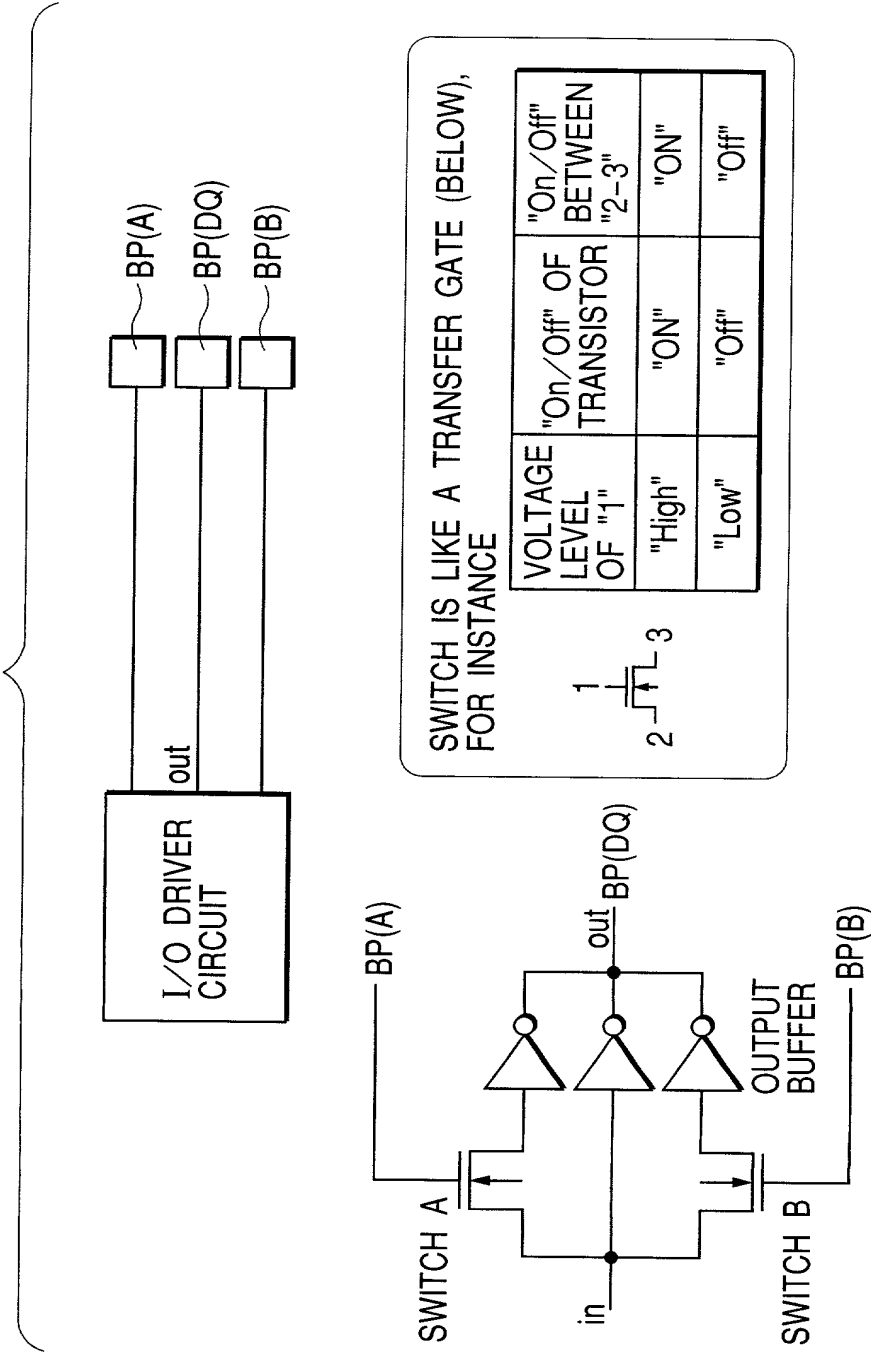


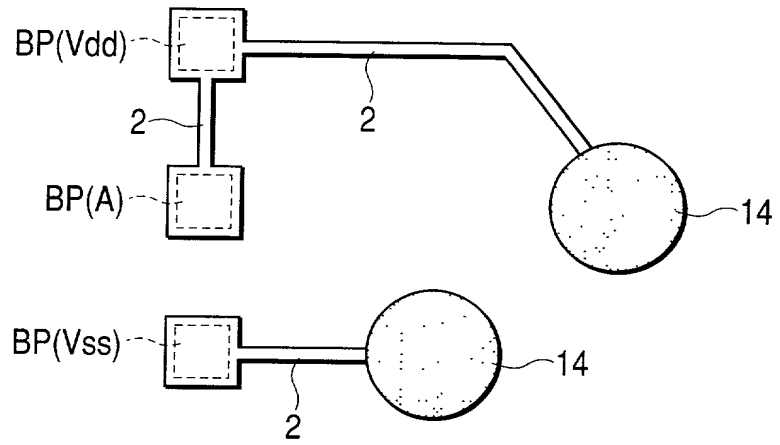
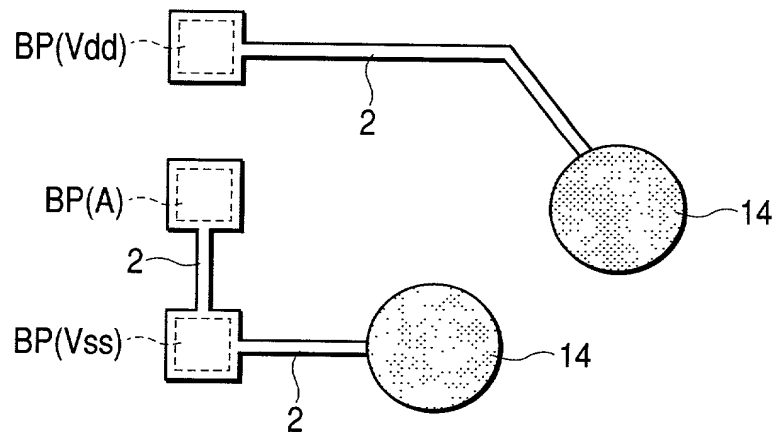
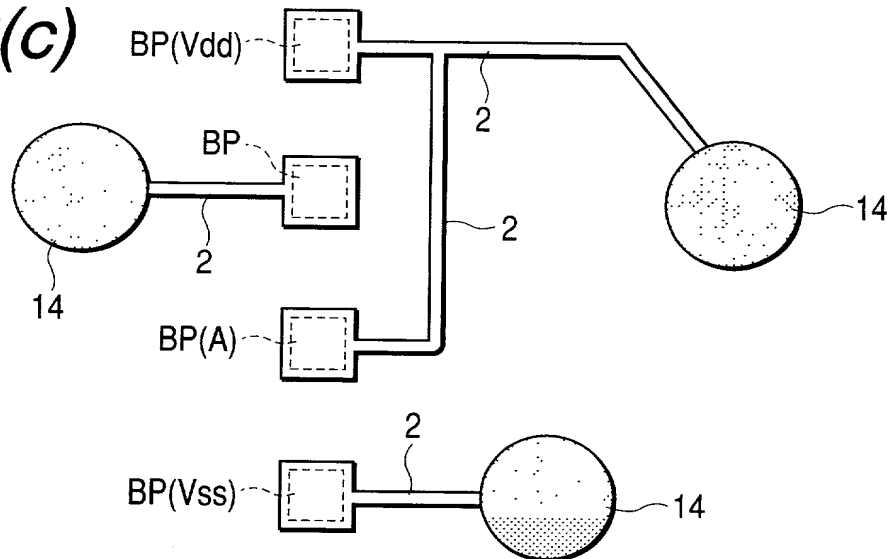
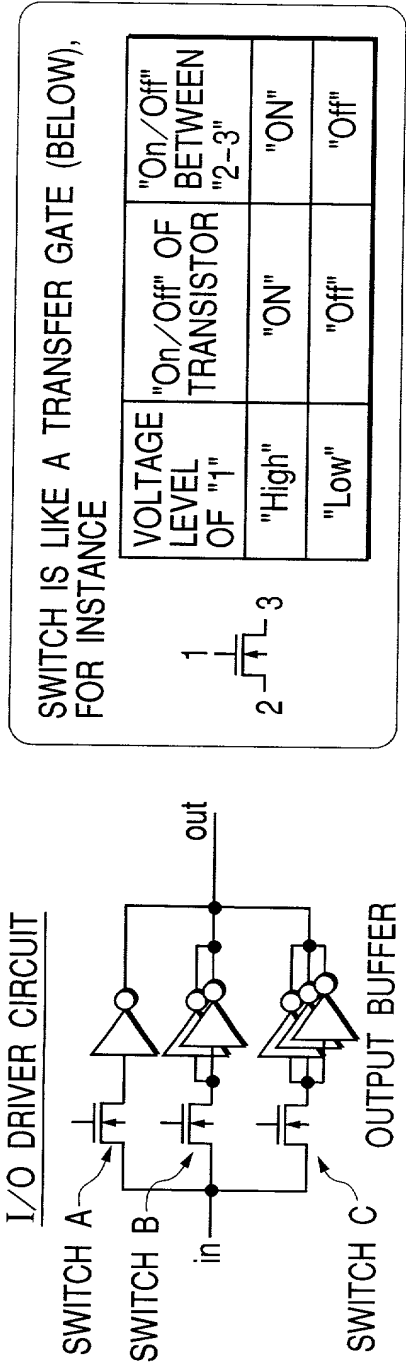
FIG. 46(a)**FIG. 46(b)****FIG. 46(c)**

FIG. 47



On/Off OF EACH TRANSISTOR (A/B/C)	RATIO OF DRIVERABILITY
"On/Off/Off"	x1
"Off/On/Off"	x2
"Off/Off/On"	x3
"On/Off/On"	x4
"Off/On/On"	x5
"On/On/On"	x6

FIG. 48(a)

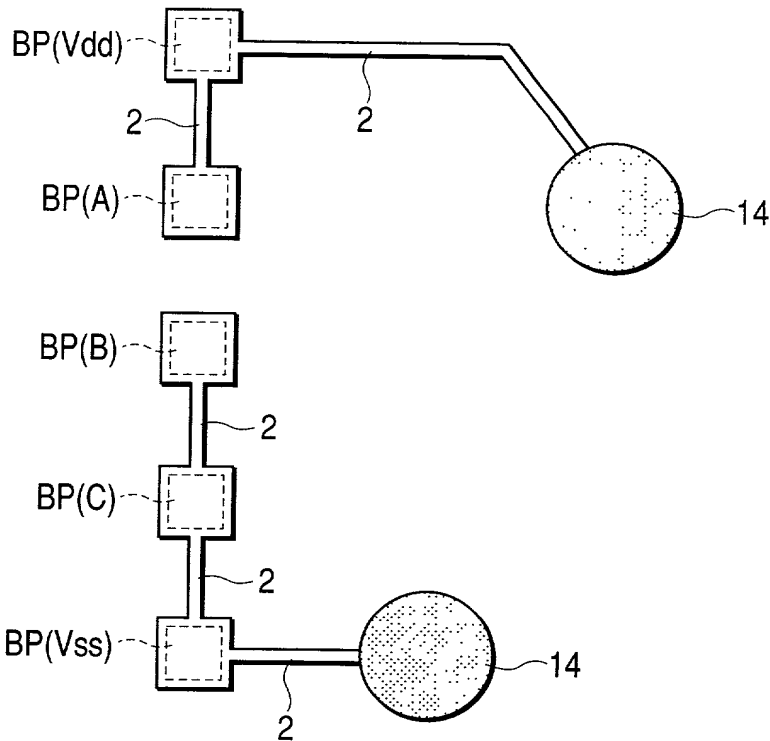


FIG. 48(b)

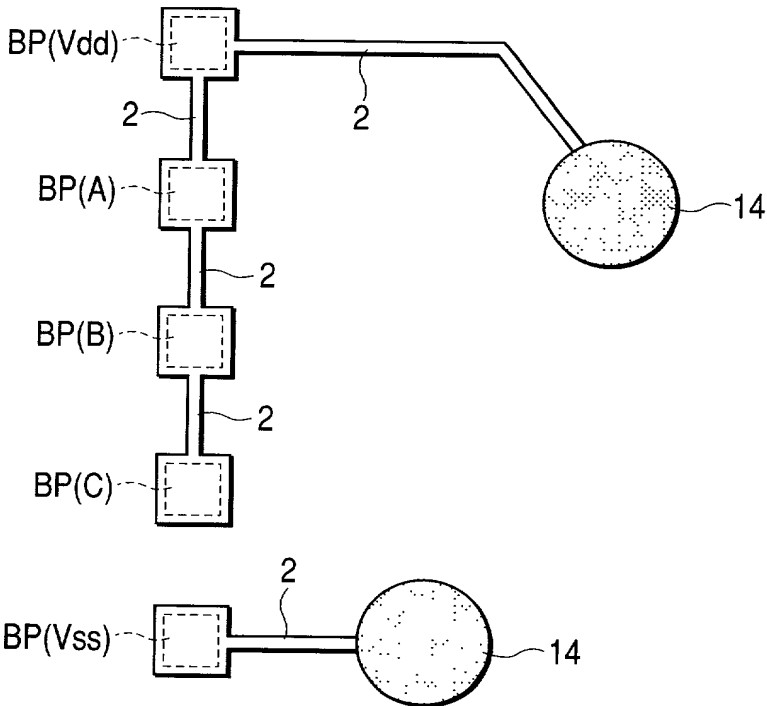
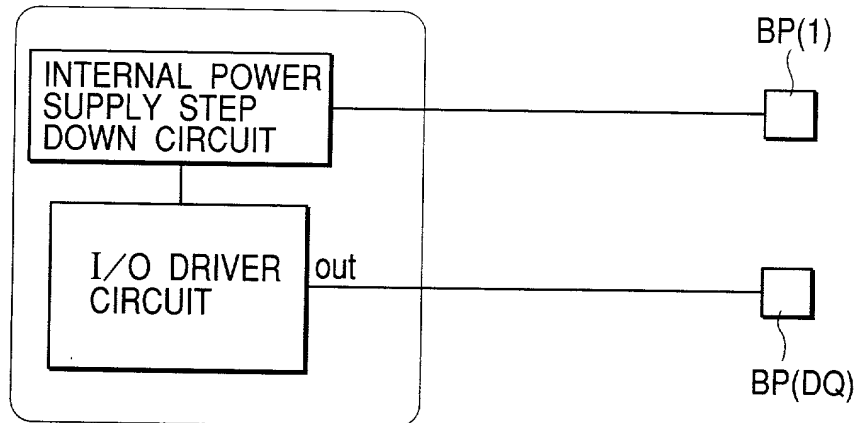
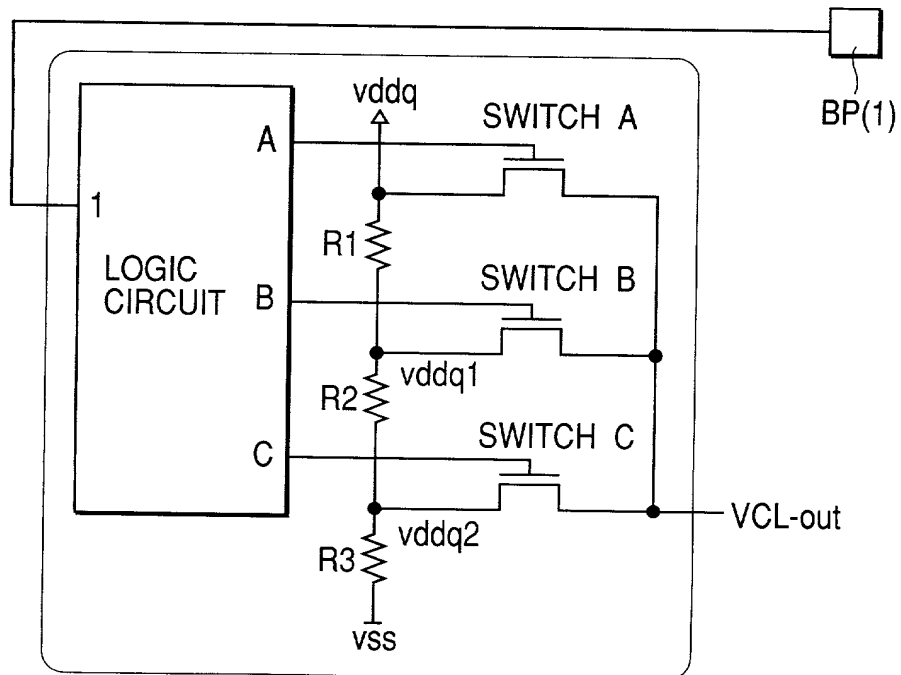


FIG. 49

VARIABLE VOLTAGE AMPLITUDE
CIRCUIT FOR I/O BUFFER

FIG. 50

INTERNAL POWER SUPPLY STEP DOWN CIRCUIT

FIG. 51

VOLTAGE LEVEL AT "1"	VOLTAGE LEVEL AT "A/B/C"	"On/Off" OF SWITCH "a/b/c"	VOLTAGE LEVEL AT "VCL-out"
"NO INPUT"	"High/Low/Low"	"On/Off/Off"	"vddq"
"High"	"Low/High/Low"	"Off/On/Off"	"vddq1"
"Low"	"Low/Low/High"	"Off/Off/On"	"vddq2"

FIG. 52

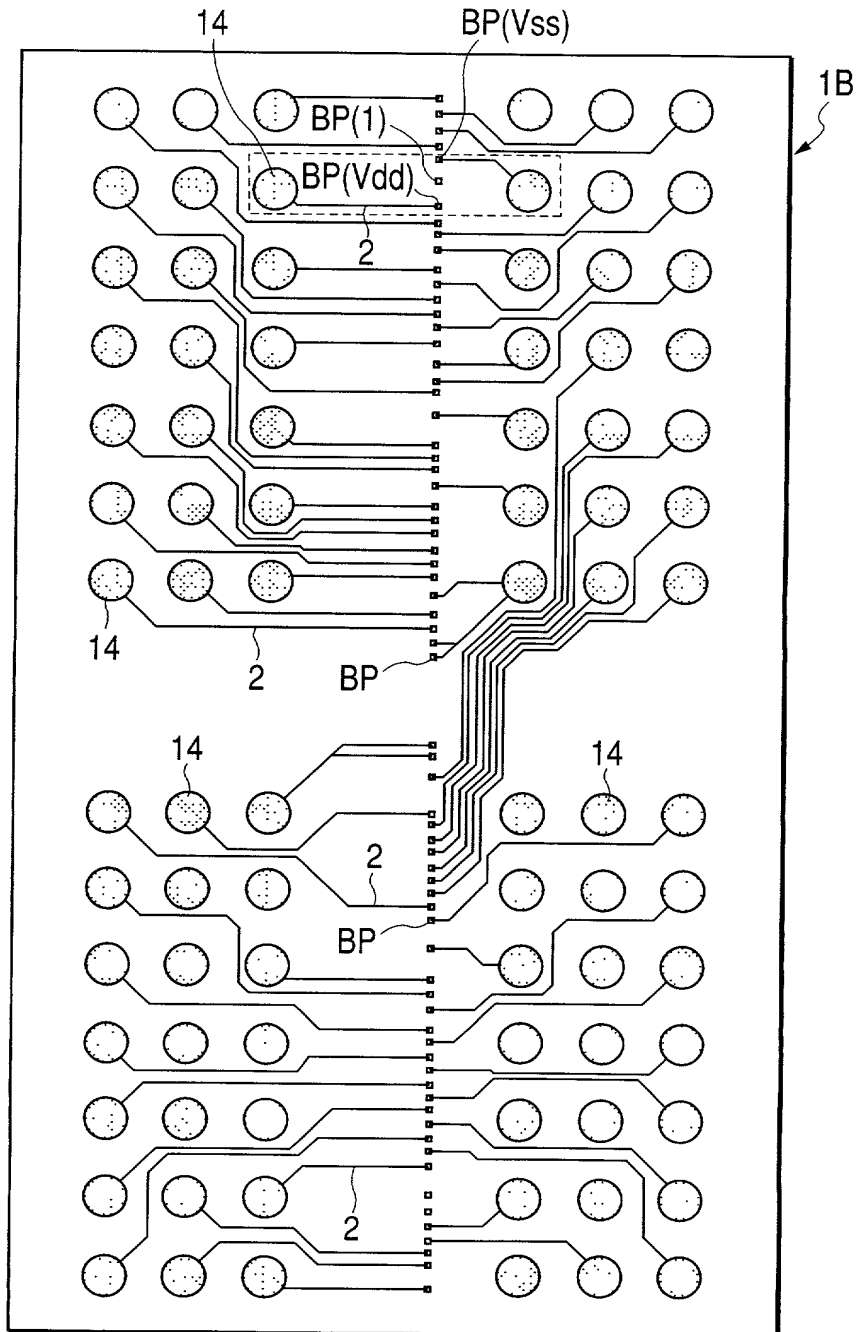


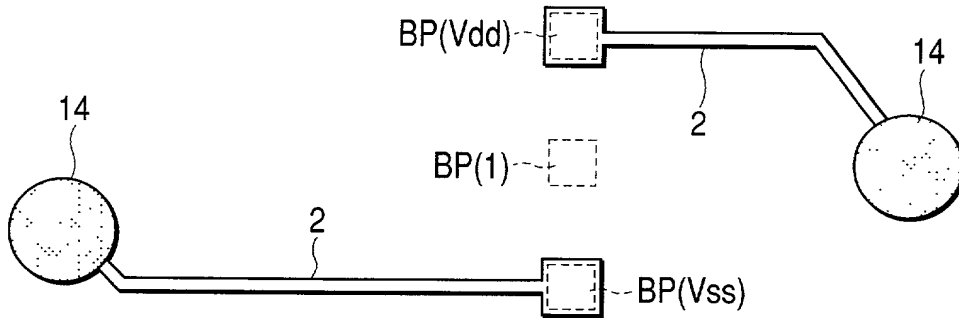
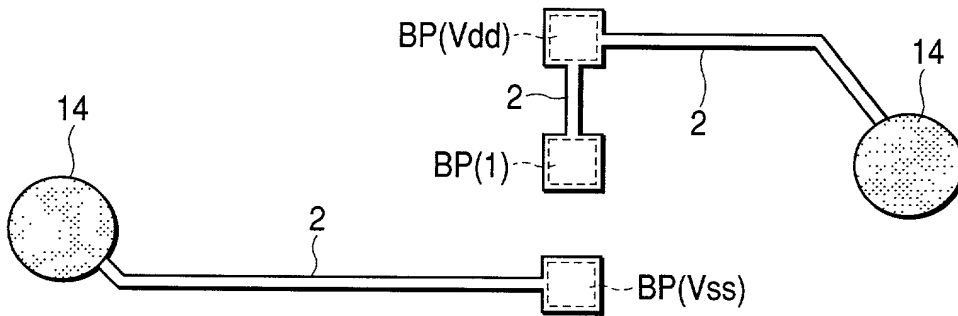
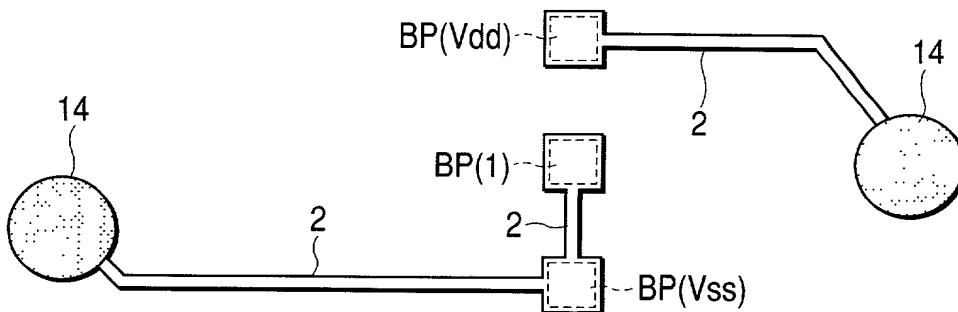
FIG. 53(a)*FIG. 53(b)**FIG. 53(c)*

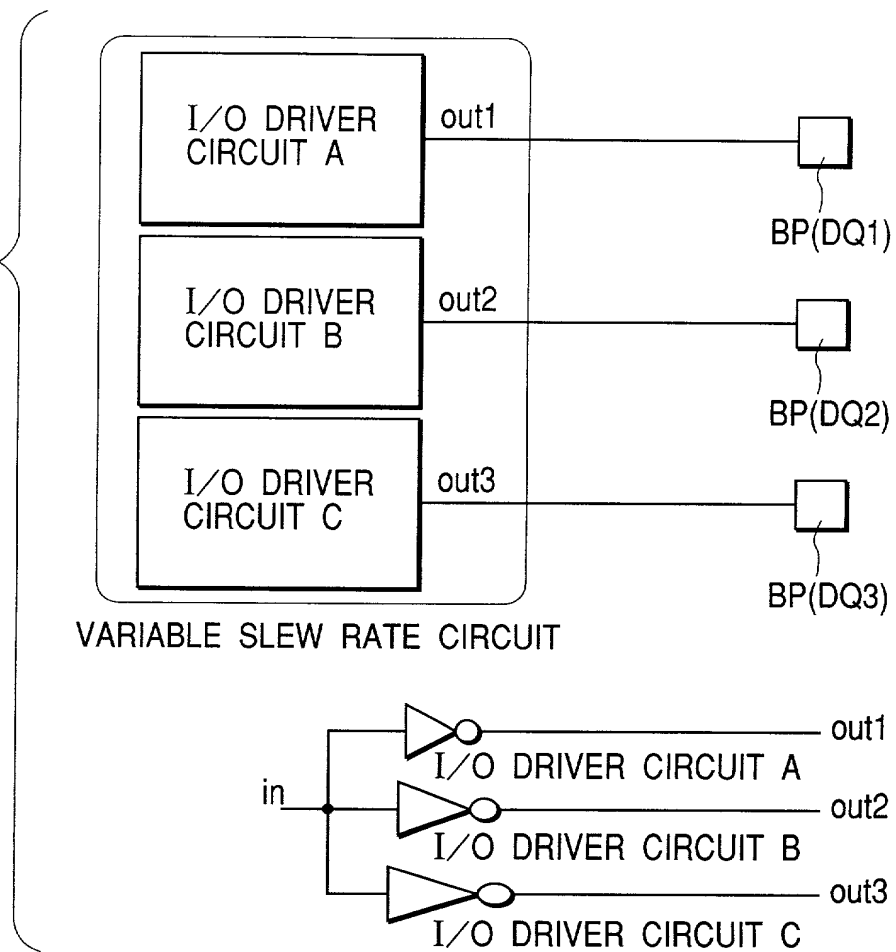
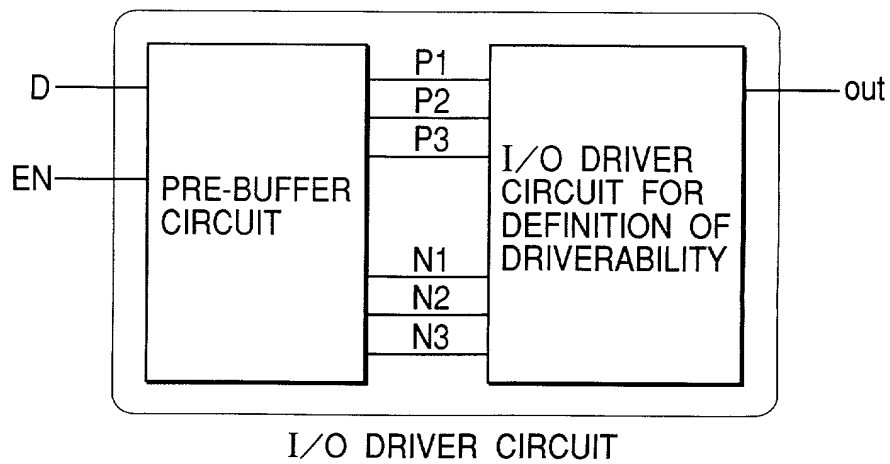
FIG. 54**FIG. 55**

FIG. 56

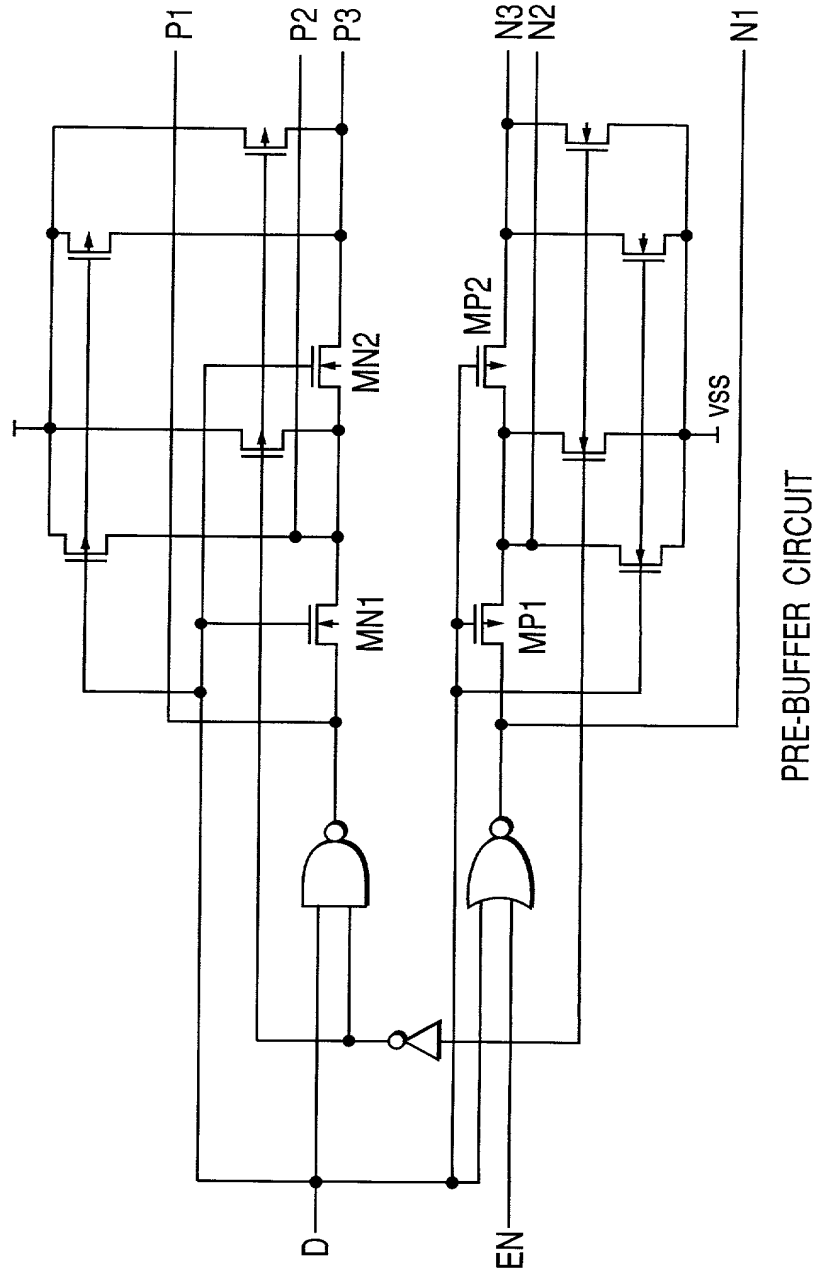
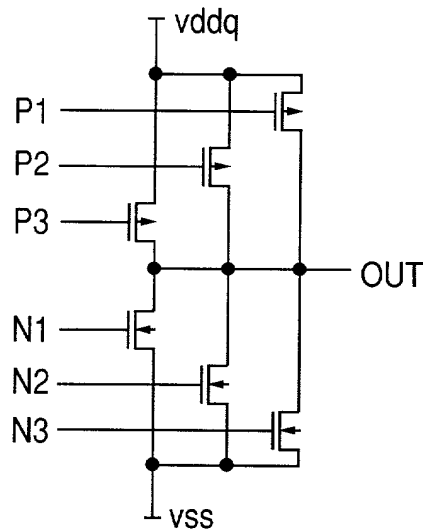


FIG. 57

I/O DRIVER CIRCUIT FOR
DEFINITION OF DRIVERABILITY

FIG. 58

W/L RATIO OF MP1 AND MP2	W/L RATIO OF MN1 AND MN2	SLEW RATE
5/1	5/2	×1 (I/O DRIVER CIRCUIT A)
5/2	5/4	×2 (I/O DRIVER CIRCUIT B)
5/3	5/6	×3 (I/O DRIVER CIRCUIT C)

THE BIGGER THE SLEW RATE IS THE SMOOTHER
THE WAVE FORM.

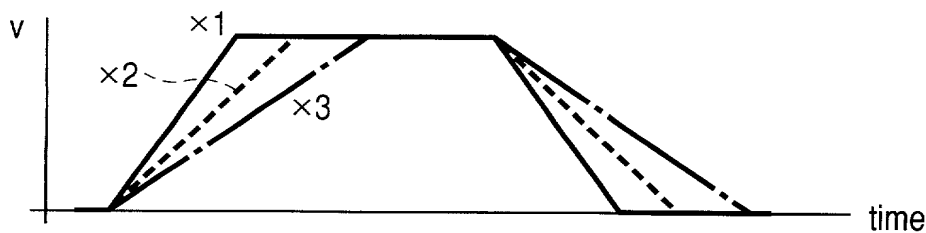


FIG. 59

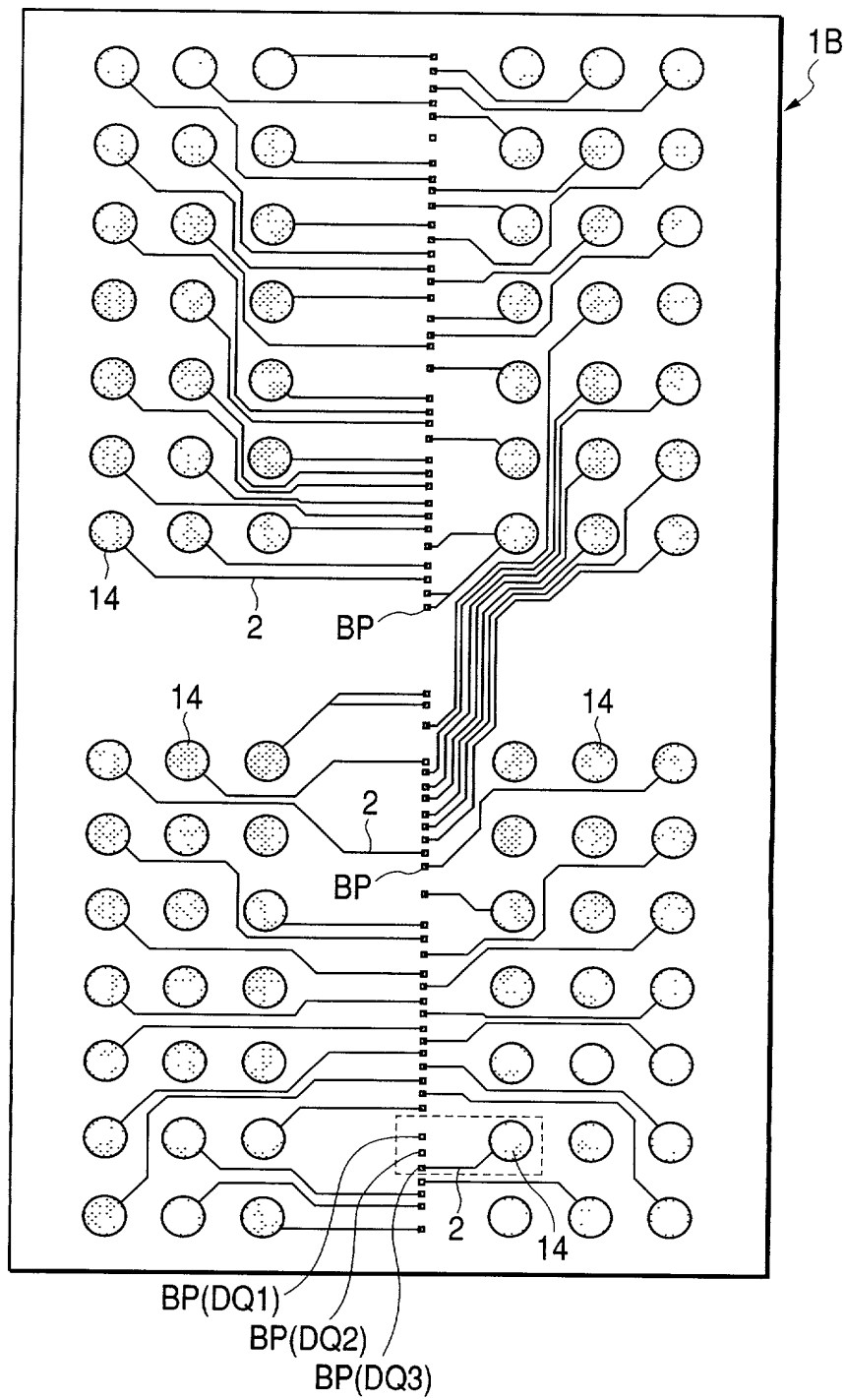


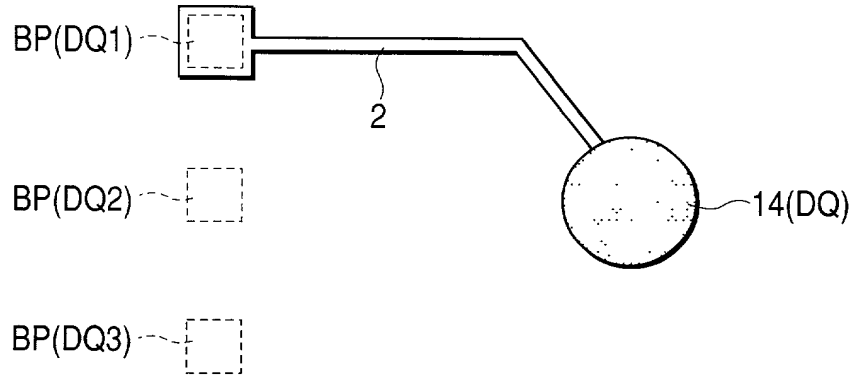
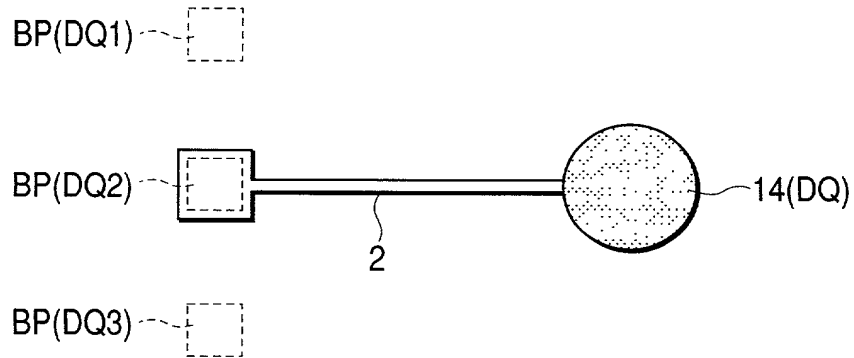
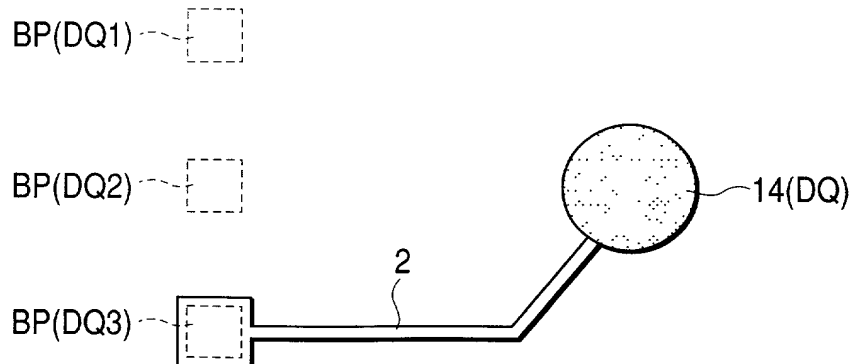
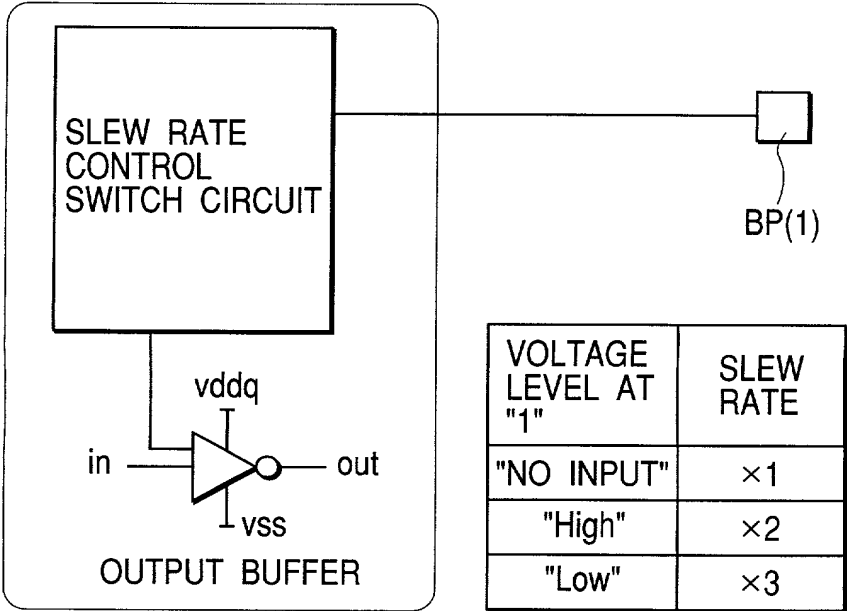
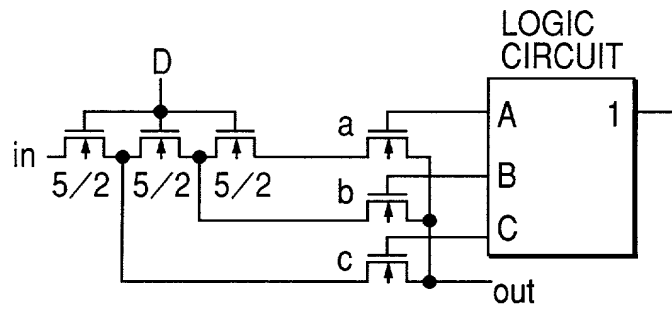
FIG. 60(a)**FIG. 60(b)****FIG. 60(c)**

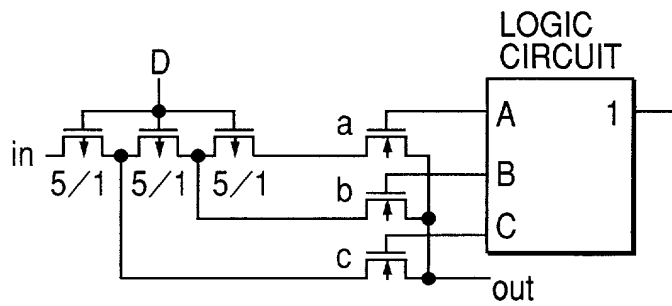
FIG. 61



VARIABLE SLEW RATE CIRCUIT

FIG. 62(a)

SLEW RATE CONTROL SWITCH CIRCUIT

FIG. 62(b)

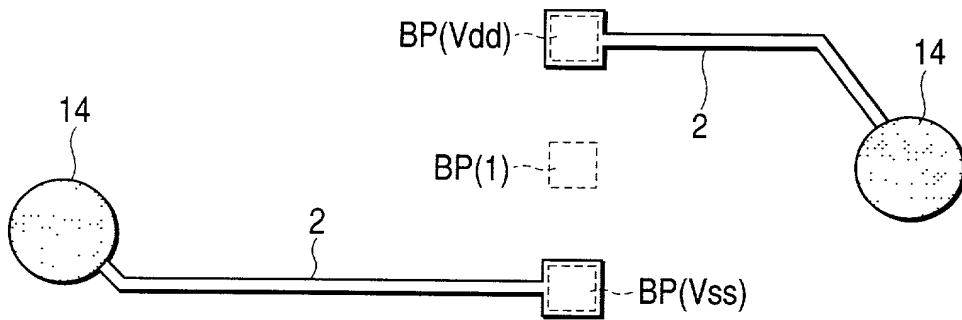
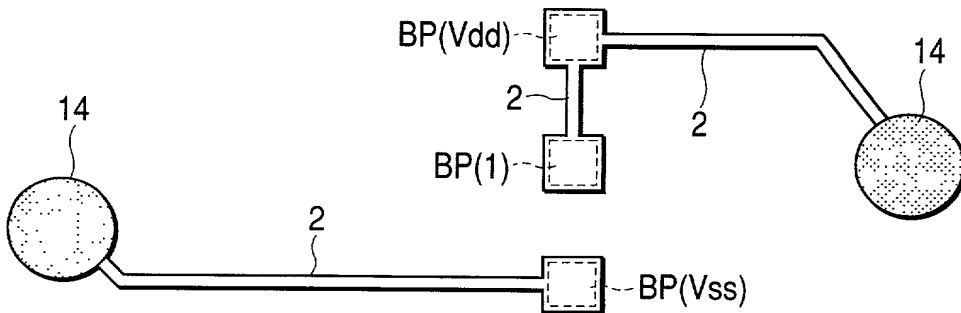
SLEW RATE CONTROL SWITCH CIRCUIT

FIG. 63

LOGIC DIAGRAM FOR LOGIC CIRCUIT (TABLE)

VOLTAGE LEVEL OF "1"	VOLTAGE LEVEL AT "A/B/C"	"On/Off" OF SWITCH "a/b/c"	SLEW RATE
"NO INPUT"	"High/Low/Low"	"On/Off/Off"	$\times 1$ (I/O DRIVER CIRCUIT A)
"High"	"Low/High/Low"	"Off/On/Off"	$\times 2$ (I/O DRIVER CIRCUIT B)
"Low"	"Low/Low/High"	"Off/Off/On"	$\times 3$ (I/O DRIVER CIRCUIT C)

THE BIGGER THE SLEW RATE IS THE SMOOTHER THE WAVE FORM.

FIG. 64(a)*FIG. 64(b)**FIG. 64(c)*